National Exams December 2017

98-Comp-A3, Computer Architecture

3 hours duration

NOTES:

1. If doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumptions made.

2. This is an OPEN BOOK EXAM.
   Any approved Casio or Sharp calculator is permitted.

3. FIVE (5) questions constitute a complete exam paper.
   The first five questions as they appear in the answer book will be marked.

4. Answering questions 1 and 2 is mandatory.

5. The questions are not of equal value.

6. Some questions require an answer in essay format. Clarity and organization of the answer are important.

Marking Scheme

1. (a) 5 marks (b) 5 marks (c) 5 marks
2. (a) 5 marks (b) 5 marks (c) 5 marks (d) 5 marks
3. (a) 5 marks (b) 5 marks (c) 5 marks
4. (a) 5 marks (b) 10 marks
5. (a) 5 marks (b) 10 marks
6. (a) 10 marks (b) 10 marks

1. **(a)** What is a structural hazards in a pipelined processor? What is a data hazard in a pipelined processor. Would a 2-way superscalar processor that is also pipelined encounter more data hazards than a single-issue pipelined processor? Explain your answer.

   (b) A processor executes a sequence of 40 instructions out of which only 10 are memory reads and one is a memory write. Each of these memory reads or writes accesses 4 bytes of memory data. Each instruction is encoded using 32 bits. What is the minimum number of bytes that a processor will have to read from memory when it executes these 40 instructions?

   (c) A processor's memory contains the value 0x0000 FFAB at address 0x1000 1004. What can this value be? An instruction? Data? Either?

2. **(a)** Two 16-bit registers A and B contain the values 0xFFF0 (shown in hexadecimal) and 0x0010, respectively. What is the value of A + B in **decimal**, if (i) A and B were to be interpreted as unsigned integers, and (ii) if A and B were to be interpreted as signed integers in 2's complement. Explain your answer.

   (b) If A and B are unsigned integers represented using 32 bits, can A x B always be represented in the same representation? Explain your answer with an example if appropriate.

   (c) The IEEE standard for single precision floating point representation of real numbers uses 32-bits in total comprising an 8-bit exponent E, a sign bit S, and a 23 bit mantissa M. The number encoded is:

   $(-1)^S \times 2^{(E - 128)} \times 1.M$

   Given three floating point numbers A, B, and C does the following equation hold? (A + B) x C = (A x C) + (B x C). Explain your answer.

   (d) Explain how a two dimensional array A of 32-bit values having 16 rows and 8 columns will be stored in memory. Where in memory would be A[R][C] if the array is stored starting from memory address 0x2000?

3. **(a)** A processor has a 4GB byte-addressable address space. How will a 48KB, 3-way set-associative cache with 32-byte blocks be indexed. Explain your answer.

(b) A block cached in set 0x10 (hexadecimal) of the cache described in part (a) is tagged with 0x01 (hexadecimal). What is the range of addresses it contains in hexadecimal?

(c) A processor performs a sequence of 100 memory reads each reading a byte from memory. The processor has a data and an instruction cache, each using 16 byte blocks. Assume that all instruction fetch accesses are hits in the instruction cache and that the data cache is empty. On a miss, the data cache fetches a complete 16-byte block from memory. What is the minimum number of bytes that the data cache will have to read from memory to service all 100 memory reads? What is the maximum?

4. **(a)** In the following assembly code identify all RAW (read-after-write), WAR (write-after-read) and WAW (write-after-write) dependencies:

```
I0     L: lw $2, 0($2)      # $2=MEM[$2+0]
I1        beq $2, $0, D     # if ($2==0) PC=D
I2        lw $3, 4($2)      # $3 = MEM[$4+4]
I3        beq $3, $5, E     # if ($3 == $5) PC=E
I4        beq $0, $0, L     # if ($0 == $0) PC = L
I0a    L: lw $2, 0($2)
I1a       beq $2, $0, D
I2a       lw $3, 4($2)
I3a       beq $3, $5, E
I4a    E: sw $2, 0($3)      # MEM[$3+0]=$2
```

$0-$31 are registers. Mark dependencies as (x,y,rz) pairs where x and y code labels and where y depends on x through register rz. Make sure to specify the dependency type, e.g., RAW (I0, I1, $2).

(b) A processor has an L1 data cache with a 3-cycle latency and an average 96% hit rate. Main memory latency is 80 cycles. If an L2 data cache is added with a 12-cycle latency what should be the L2 hit rate so that the average memory latency as observed by the processor is lower than with just the L1 cache? When an L2 cache is added, it will have to be accessed on L1 misses before accessing main memory. State your assumptions and explain your answer.

5. **(a)** A memory chip has the following interface: A0-A14 are 15 single bit input address lines specifying which row is accessed, a single bit input signal R/W! specifies whether the access is a read (1) or a write (0), E is a single bit input signal that must be 1 to access the chip. The data values that are read or written appear on the two D1 through D0 single bit output/input pins. When E is 0 the D1-D0 pins are in high-Z. What is the total capacity of this memory chip in bytes?

(b) Using as many as necessary of the chips described in part (a), synthesize the equivalent of an 8-bit wide memory that has a 32KB total capacity. You can use a few additional logic gates as needed.

6. **(a)** The following code can be rescheduled by the compiler or the programmer to avoid the load-use stalls on a 5-stage pipeline. Show a schedule that avoids these load-use stalls. Loads produce their value in the 4 stage whereas ADD instructions need their value at the beginning of their 3rd stage.

```
lw $5, 0($4)   # $5=MEM[$4+0]
lw $6, 4($4)   # $6=MEM[$4+4]
add $6, $5, $6# $6=$5+$6
sw  $6, 0($7) # MEM[$7+0]= $6
lw $8, 8($4)# $8=MEM[$4+8]
lw $9, 12($4) # $9=MEM[$4+12]
add $9, $8, $9# $9=$8+$9
sw $9, 0($10) # MEM[$10+0]=$9
```

(b) Consider the following hypothetical instruction encodings for an 8-bit CPU design that has four general purpose registers $0 through $3.

Instruction	Instruction Encoding – Bits 7-0							
	7	6	5	4	3	2	1	0
Load R1 (R2)	R1		R2		0	0	0	0
Store R1 (R2)	R2		R1		0	0	1	0
Add R1 R2	1	0	0	0	R1		R2	
BZ Imm4	Imm4				0	1	0	1

R1 and R2 are 2-bit fields that identify one of the four general purpose registers. Imm4 is a 4-bit immediate field.

What problems arise from this encoding? Which encodings would you change? Justify your answer.