National Exams **May 2016**

98-Comp-A2, Digital Systems Design

3 hours duration

NOTES:

1. If doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumptions made.

2. This is a Closed Book exam.
   Candidates may use one of two calculators, the Casio or Sharp approved models.

3. FIVE (5) questions constitute a complete exam.

4. All questions are worth 20 points

Marking Scheme

1. (1.1) 2, (1.2) 2, (1.3) 2, (1.4) 2, (1.5) 2, (1.6) 2, (1.7) 2, (1.8) 2, (1.9) 2, (1.10) 2 total = 20
2. (a) 10, (b) 10, total = 20
3. (a) 10, (b) 10, total = 20
4. (a) 15, (b) 5, total = 20
5. (a) 7, (b) 7, (c) 6, total = 20
6. (a) 5, (b) 5, (c) 5, (d) 5, total = 20

The number beside each part above indicates the points that part is worth

1) Circle the letter of the best answer (20 points)

1.1 Synchronous digital logic means: [2 pts]

A. All gates are triggered at the same time
B. All flip-flops are triggered at the same time
C. All events occur at the same time

1.2 Tristate signals can be described as [2 pts]

A. having three strong levels of voltage
B. having three kinds of circuits
C. having two voltages and one high impedance

1.3 A binary counter of four flip-flops has how many states? [2 pts]

A. 8
B. 15
C. 16

1.4 A read-only memory can be used for [2 pts]

A. implementing a logic function
B. implementing a register
C. implementing a read-write memory

1.5 In synchronous design rules, asynchronous flip-flop inputs are: [2 pts]

A. never used
B. used to help optimize logic
C. only used for initialization

1.6 Simulation is primarily used to: [2 pts]

A. Create the circuitry for the ASICs or FPGAs
B. Infer gates and flip-flops from the HDL
C. Verify the functionality of the design versus the requirements

1.7 The term concurrent means [2 pts]

A. occurring at different times or places
B. occurring at the same time
C. occurring at the same place

1.8 What is the primary concurrent statement used in structural architectures? [2 pts]

A. component configuration
B. component instantiation
C. component specification

1.9 The reserved word "others" does NOT mean: [2 pts]

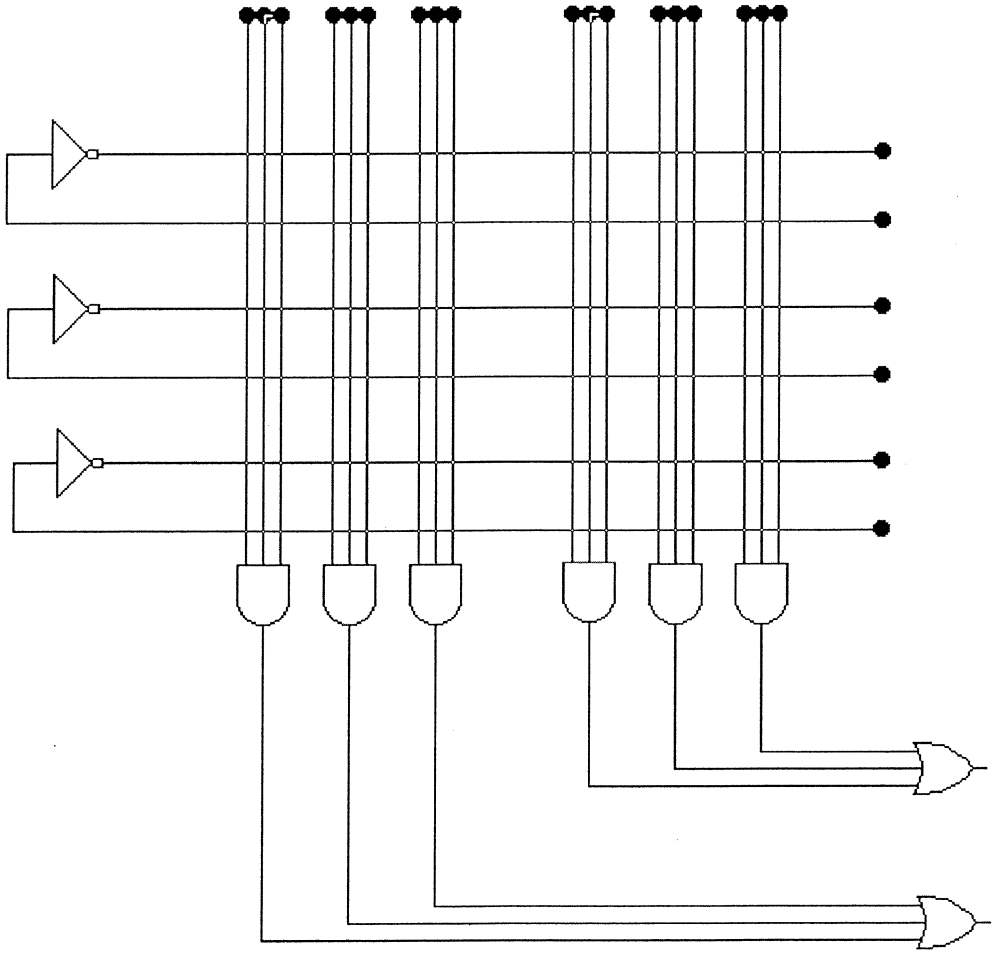
A. All elements of an array
B. All remaining values of an object
C. All statements in a model

1.10 A sensitivity list for a process inferring flip-flops contains [2 pts]

A. The clock or clock and reset
B. All inputs
C. All outputs

2). Use a PAL to implement the following two functions

F1=a'b+ab'+c [10 pts]
F2=a'b'c'+abc'+a'bc [10 pts]



3).

a. **Fill in following function into Variable entered Map.** [10 pts]

$$F = \overline{B}\overline{C}EFH + BC\overline{D}EH + \overline{B}CEHF + ABCEH\overline{G} + BCEH + A\overline{B}C\overline{E}\overline{H}$$

b. **Fill F1 into the Variable entered map and read it out** [10 pts]

A	B	C	D	F1
0	0	0	0	Φ
0	0	0	1	Φ
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	Φ
0	1	1	1	0
1	0	0	0	Φ
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	Φ

C \ AB	00	01	11	10
0				
1				

C \ AB	00	01	11	10
0				
1				

4). A circuit is needed to start and stop counting clock pulses on command.

(a) Design a 4-bit synchronous counter that goes through the sequence 0000, 0001, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001, 1010, 1011, 1100, 1101, 1110, 1111 and then repeats. Use positive-edge-triggered JK flip-flops. Label the bits Q_D, Q_C, Q_B & Q_A where Q_D is the most significant bit. Draw the circuit implementing the counter. [15 pts]

(b) Modify the circuit so that it counts whenever an additional COUNT ENABLE (CTE) input is HIGH, stops counting when CTE goes LOW and resumes counting from where it stopped when CTE goes HIGH again. [5 pts]

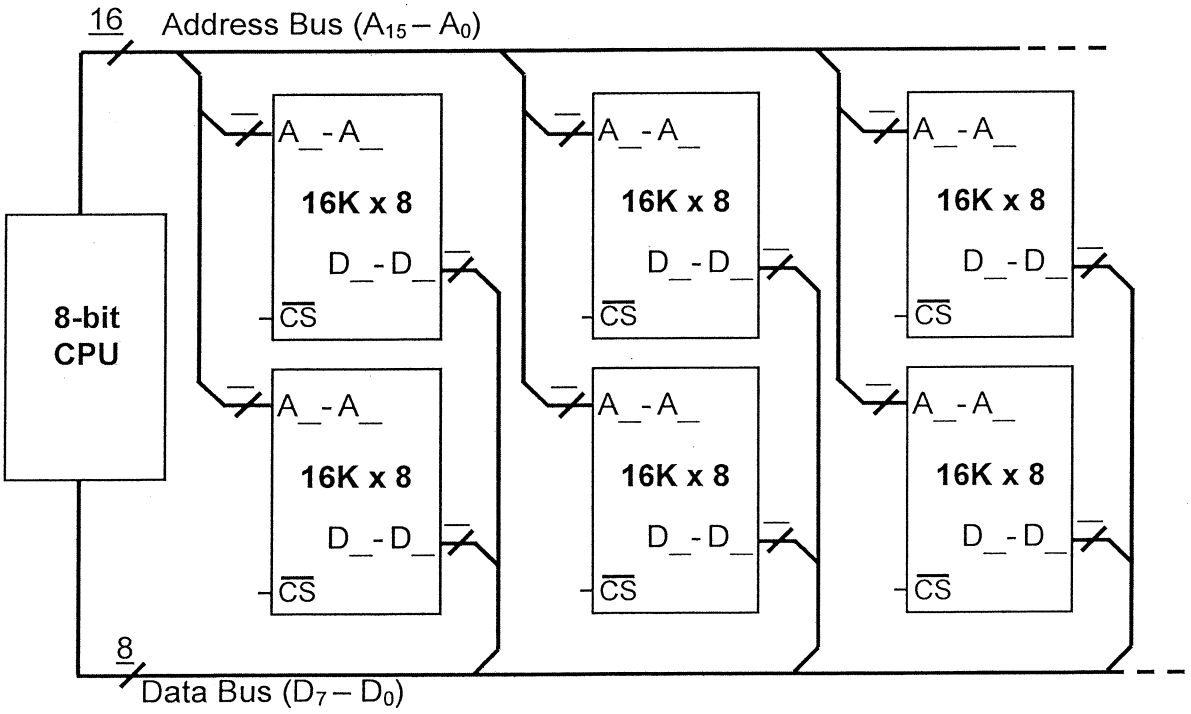
5). Provide this 8-bit CPU with a 64Kbyte memory space by making use of 16K x 4 memory chips like the ones provided in the figure below.

(a) Fill in the blanks *beside* and *inside* the memory chips with the appropriate numbers. The number on top of this symbol ⟋ represents the number of lines on that bus. The spaces besides the A's and the D's are to indicate which lines of the address and data busses are connected to each chip, respectively. [7 pts]

(b) Complete the connections in the figure below adding logic gates where needed to produce the chip select ($\overline{CS}$) signals needed in the decoding logic. Explain the reasons for the connections made, include expressions for the Boolean logic used. [7 pts]

(c) Provide the address range allocated to each of the chips used. [6 pts]

Note: R/$\overline{W}$ & clock signals are omitted for simplicity.



6).

A) Why are interrupts useful? [5 pts]

B) Why interrupts should be prioritized? [5 pts]

C) How to handle the interrupts [5 pts]

D) What is the difference between maskable interrupts and nonmaskable interrupts? [5 pts]