National Exams December 2017

04-BS-8, Digital Logic Circuits

3 hours duration

NOTES:

1. If a doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumption made with the answer of the question.

2. Candidates may use one of two calculators, the Casio or Sharp approved models. This is a closed book examination; however, candidates are allowed to bring one hand-written information sheet (8.5" X 11") of self-prepared notes.

3. This paper contains **FIVE (5)** questions and comprises **six (6)** pages.

4. Any **FOUR (4)** questions constitute a complete paper. Only the first four questions as they appear in your answer book will be marked.

5. All questions are of equal marks. Total marks = 100.

6. Each question carries 25 marks and the marks for each part of the questions are indicated in brackets.

7. A PAL16L8 Data sheet is provided in the Appendix. It can be used to provide the solution of Question 4, part (c) and should be attached to your answer sheet.

1. Design a synchronous counter that has the following sequence: 0, 1, 3, 5, 7, 9, 11, 13 and repeat. The unused states must always go to 0 state on the NEXT clock pulse. Use positive edge triggered D-type flip-flops and standard logic gates to implement your design.

(a) Start your design with a state table.

(5 marks)

(b) Develop the next state equations and simplify them if required. Show your complete work.

(13 marks)

(c) Implement and draw the synchronous counter circuit.

(7 marks)

2. A combinational logic circuit is required to divide a 4-bit binary number $(A_3A_2A_1A_0)_2$ by a constant 4 as shown in Figure P2. There are two outputs of the circuit i.e. **Q**uotient and **R**emainder.

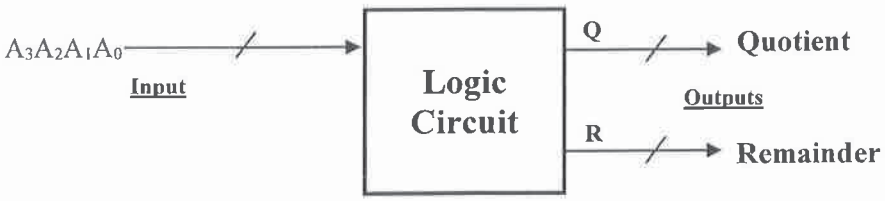


Figure P2

(a) Determine the size of input and outputs in terms of bits.

(4 marks)

(b) Construct the truth table of the circuit indicating the input and output variables along with their sizes.

(7 marks)

(c) Simplify each output function using K-maps, and write the reduced Boolean functions of each output (Q_x and R_y).

(8 marks)

(d) Implement the combinational logic circuit developed in part (c) by using minimum number of gates.

(6 marks)

3. (a) Briefly answer the following questions:

- Determine a 2's complement representation for the negative decimal number 10,000 or $(-10{,}000)_{10}$. Use suitable number of bits.
- Determine the minimum number of gates required to implement a single-bit Full adder. You can use only AND, OR and XOR gates.

(3+3 marks)

(b) Determine the clocked flip-flop described in the following excitation table, where x represents don't care conditions.

Qn	Qn+1	Inputs A	Inputs B
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0

(6 marks)

(c) Consider the following logic function **F**.
F(w, x, y, z) = $\sum$m(0, 2, 3, 5, 6, 9, 13).

(i) Write the Boolean equation for function **F**, and simplify it by using Boolean algebra only. Show your complete work.

(ii) Implement the function **F** by using minimum number of NAND gates only.

(8+5 marks)

4. A small corporation has 13 shares of stock, and each share entitles its owner to one vote at the stockholder's meeting. Three people own 13 shares of stock as follows:

Bob (B): 4 shares
Chris (C): 6 shares
Dave (D): 3 shares

Each stockholder must close a switch when voting *yes* and open it when voting *no* for his/her shares as shown in Figure P4. The outputs of the voting logic circuit present the total number of shares that vote *yes* for each measure.

(a) Represent the voting logic circuit problem in terms of a truth table.
(5 marks)

Question #4 continues on Page 4

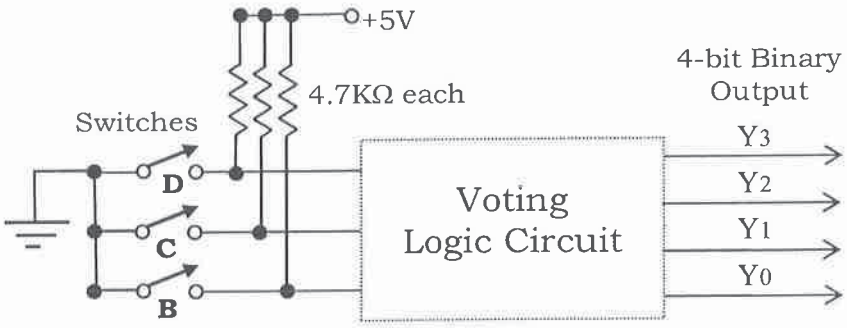


Figure P4

4. (b) Develop and simplify the Boolean expressions for all the outputs of voting logic circuit.

(12 marks)

(c) Implement the voting logic circuit by using a PAL16L8 device given in the appendix. Show the intact PAL fuses by crossing them in the diagram and attach it to your answer book.

(8 marks)

5. (a) How a Toggle flip-flop can be constructed by using a JK flip-flop and some logic gates. Draw the complete diagram of the circuit.

(4 marks)

(b) Design and draw a sequential circuit using D-type flip-flops that produce a 15MHz frequency signal with 50% duty cycle from a 60MHz clock signal with 25% duty cycle. Draw the input and output of your circuit for a few clock cycles.

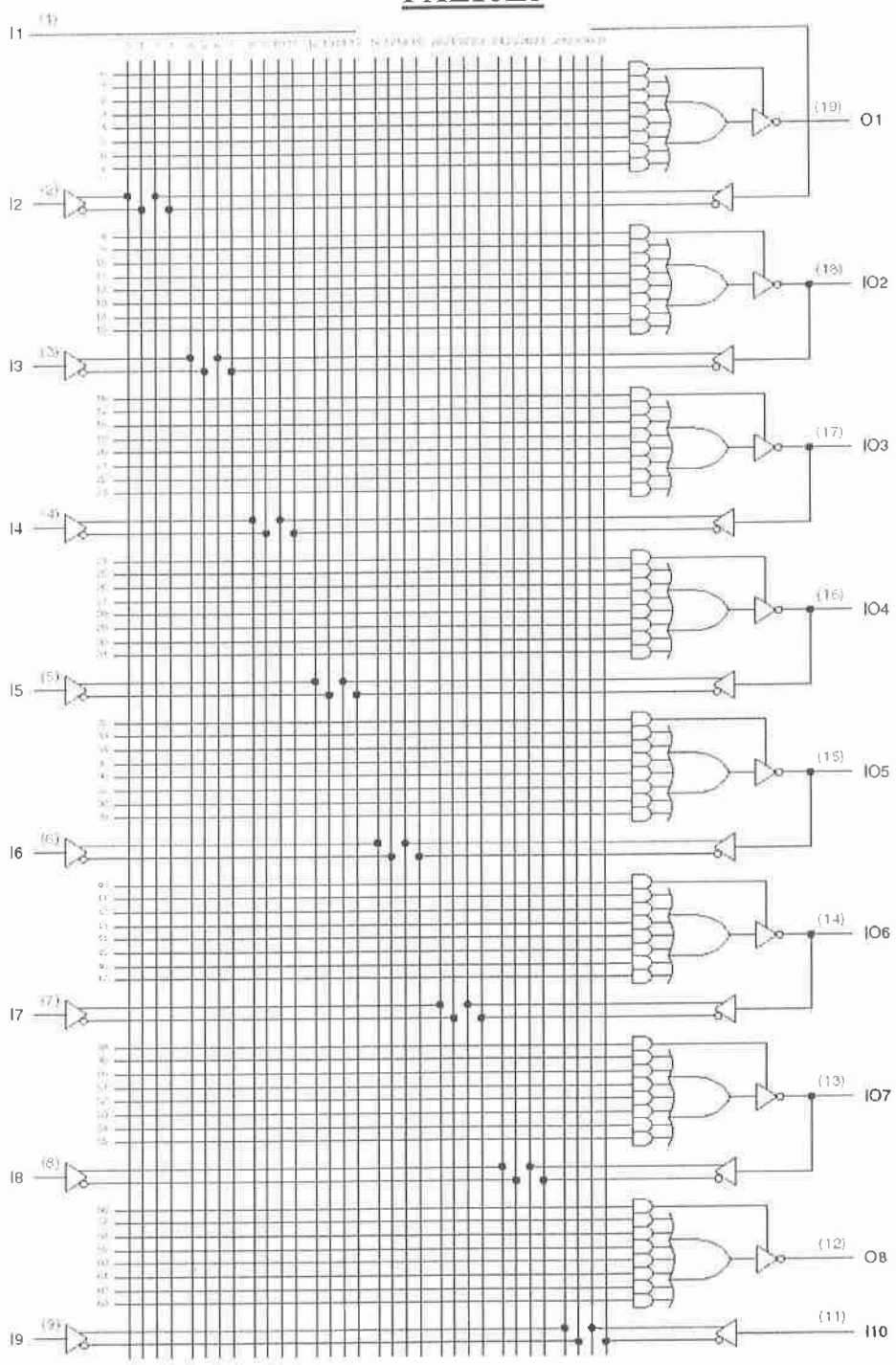
(7 marks)

(c) Develop and draw a sequential circuit that converts an 8-bit binary number to 2's complement form. Assume that the input binary number is loaded in an 8-bit shift register. After eight clock cycles, the shift register has the converted binary number. You can use a suitable type Flip-Flop with some logic gates.

(14 marks)

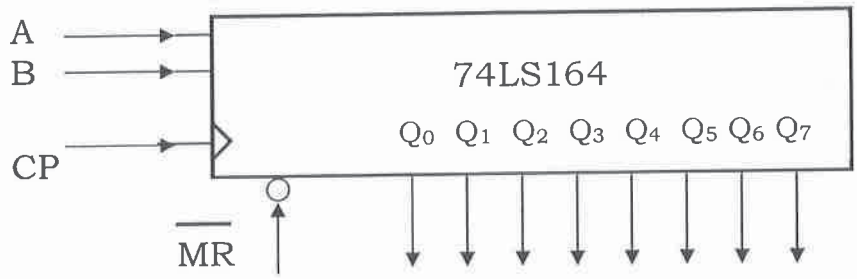
APPENDIX

PAL16L8



Counter and Decoder Data Sheets

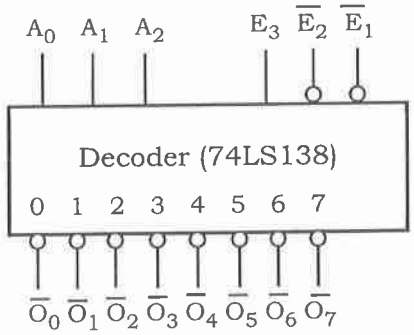
74LS164: 8-bit Shift Register



- An eight-bit shift register with all FF outputs Q_0, Q_1, Q_2, Q_3, Q_4, Q_5, Q_6 and Q_7 are externally available.
- Inputs A and B are ANDED together to produce the serial input to flip-flop Q_0.
- Shift operation occurs at PGTs of the clock input CP.
- The $\overline{MR}$ input resets all FFs asynchronously on a LOW level.

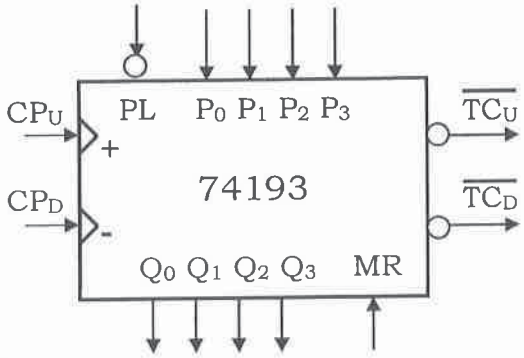
74LS138: 3-to-8 Decoder

Inputs			
$\overline{E}_1$	$\overline{E}_2$	E_3	
0	0	1	Respond to input code $A_2A_1A_0$
1	x	x	Disabled all HIGH
x	1	x	Disabled all HIGH
x	x	0	Disabled all HIGH



74193, 4-bit UP/DOWN Counter

MR	$\overline{PL}$	CP_U	CP_D		Mode
H	x	x	x		Asynch reset
L	L	x	x		Asynch Load
L	H	H	H		No change
L	H	↑	H		Count up
L	H	H	↑		Count down



End of Paper