National Exams December 2019

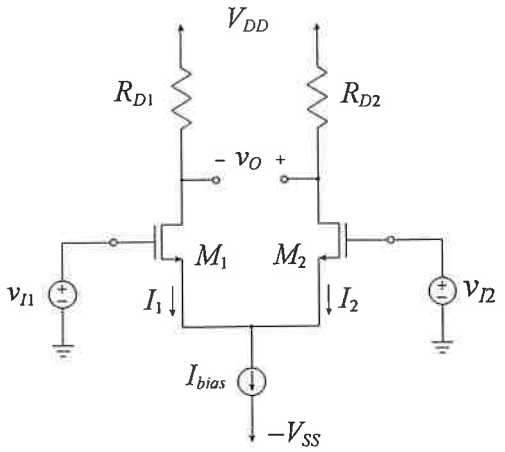
16-Elec-B5, Advanced Electronics

3 hours duration

Notes:

1. If any doubt exists as to the interpretation of any question, the candidate is urged to submit, within their answer, a clear statement of any assumptions made.
2. This is a **CLOSED BOOK EXAM.**
   A Casio or Sharp approved calculator is permitted.
3. Answer all **FIVE** (5) questions.
4. All questions are worth 20 marks each.
5. Please start each question on a new page and clearly identify the question number and part number, e.g. Q4(a).
6. In schematics, ground and chassis may be assumed to be common, unless specifically stated otherwise.
7. Unless otherwise specified, assume that Op-Amps are ideal and that supply voltages are ±15V.
8. If questions require an answer in essay format, clarity and organization of the answer are important. Provide block diagrams and circuit schematics whenever necessary.

QUESTION (1)



This differential amplifier uses a bias current of $I_{bias} = 20\ \mu A$

The two MOS transistors have
$V_{TH} = 1$ V, $W/L = 120\ \mu m/\ 6\ \mu m$, and $\mu C_{ox} = 20\ \mu A/V^2$

a) Find the values for V_{GS1}, V_{GS2}, g_{m1}, g_{m2} and the differential input voltage $v_{ID} = v_{I1} - v_{I2}$ that will cause full current switching (i.e. when either I_1 or I_2 becomes zero). (10 points)

b) If there is a 2% mismatch between R_{D1} and R_{D2}, what will be the input offset voltage? (6 points)

c) If there is a 2% mismatch in the threshold voltage between M_1 and M_2, what will be the input offset voltage? (4 points)

Useful formulae: for n-channel MOSFET

$$i_{DS} = K\left[(v_{GS} - V_{TH})v_{DS} - \frac{1}{2}v_{DS}^2\right] \quad \text{triode region}$$

$$i_{DS} = \frac{1}{2}K(v_{GS} - V_{TH})^2(1 + \lambda v_{DS}) \quad \text{saturation region}$$

$$V_{ov} = V_{GS} - V_{TH} \quad \text{overdrive voltage}$$

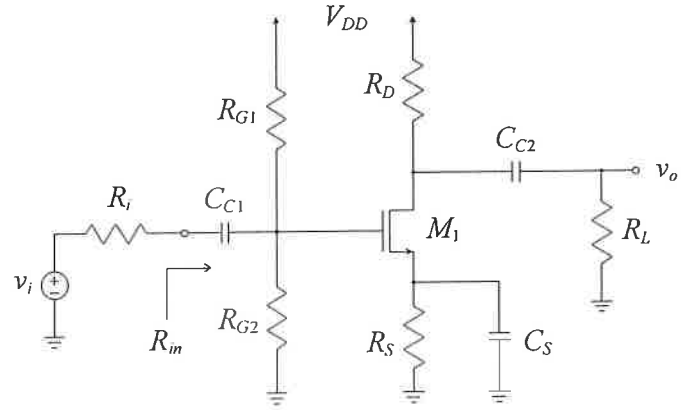
where

$$K = K'\left(\frac{W}{L}\right) = \mu C_{ox}\left(\frac{W}{L}\right)$$

$$V_A = \frac{1}{\lambda}, \text{ and } V_A = V_A' L, \ r_o = \frac{1}{\lambda I_D}$$

QUESTION (2)

In this common source amplifier, determine the mid-band gain, and also the values of the coupling capacitors, C_{C1}, C_{C2}, and C_S such that the low frequency response is dominated by a pole at 100 Hz and the nearest pole or zero will be at least one decade away. (20 points)



You can assume the following operating condition:

$V_{DD} = 20$ V	$I_D = 1$ mA
$V_{GS} = 2$ V	$V_D = +15$ V
$R_{G1} = 1.45$ MΩ	$R_{G2} = 0.55$ MΩ
$R_S = 3.5$ kΩ	$R_D = 5$ kΩ
$R_i = 100$ kΩ	$R_L = 10$ kΩ

For transistor M_1:

$V_{TH} = 1$ V	$K = 1\text{mA/V}^2$
$r_0 = \infty$	

Note: you can ignore the high frequency equivalent circuit model for M_1. (i.e. $C_{gs1} = C_{gd1} = 0$)

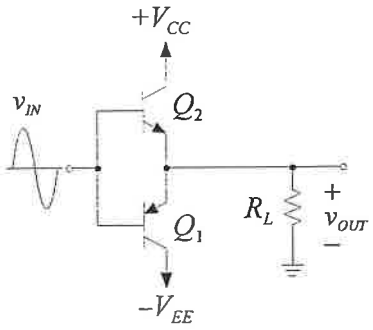
QUESTION (3)

For this class B output stage, determine

a) The maximum RMS output power. (4 points)

b) The RMS power dissipated by M1 under maximum output power. (8 points)

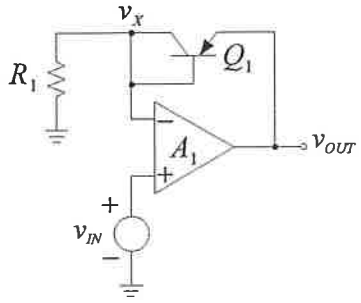
c) The power efficiency, η of this output stage. (8 points)



Given: $\beta = 50$,
$V_{BE,on} = 0.7$ V,
$R_L = 8\ \Omega$
$|V_{CC}| = |V_{EE}| = 20$ V.

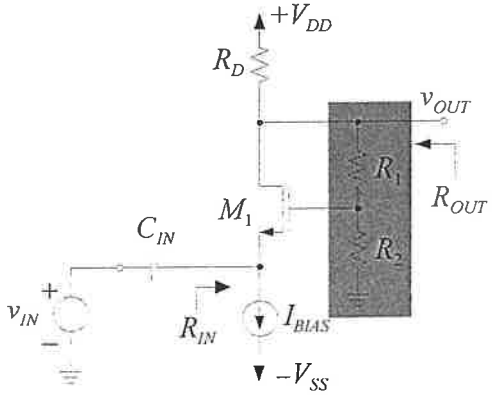
QUESTION (4)

Assuming that the op amp is ideal, derive the relationship between v_{OUT} and v_{IN}. Please note that this circuit behaves differently for positive and negative input voltages. (20 points)



QUESTION (5)

In the following is a common gate (CG) amplifier with a feedback network consisting of R_1 and R_2. Given $R_D = 2$ kΩ, $V_{DD} = 10$ V, $-V_{SS} = -10$ V, $I_{bias} = 2$ mA, and the transistor parameters as $K = 1$ mA/V^2, $V_{TH} = 1$ V, and $\lambda = 0$,



a) Determine the input and output resistance (R_{IN} and R_{OUT}) if there is no feedback network (i.e. $R_1 = \infty$, and $R_2 = 0\ \Omega$).
(8 points)

b) Derive the input and output resistance (R_{IN} and R_{OUT}) if for $R_1 = 200$ kΩ and $R_2 = 100$ kΩ.
(12 points)