National Exams December 2019

16-Mex-A2, Circuits and Electronics

3 hours duration

NOTES:

1. If doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumptions made.

2. This is a CLOSED BOOK EXAM. An approved Casio or Sharp model calculator is permitted.

3. This exam **has two parts Part A Circuits and Part B Electronics**. Answer either 3 questions from Part A and two questions from Part B or 2 questions from Part A and 3 questions from Part B a total of 5 questions answered. Indicate in the front page of your answer book which questions you want to be marked.

4. Please indicate which part the question you are answering is from ether Part A or Part B. Start each new question on a new page and number and part number e.g. Q4(a).

5. For the Part B Electronics part of the exam in schematics, ground and chassis may be assumed to be common, unless specifically stated otherwise. Also, unless otherwise specified, assume that Op-Amps are ideal and that supply voltages are ±15V.

6. If questions require an answer in essay format, clarity and organization of the answer are important. Provide block diagrams and circuit schematics whenever necessary.

7. For the Part A Circuits part of the exam some useful equations and transforms are provided.

8. All questions are of equal value. Part Marks will be given for right procedures.

16-MEX-A2

PART A

CIRCUITS

ANSWER A MAXIUM OF 3 QUESTIONS FROM THIS PART A SECTION AND TWO QUESTIONS FROM THE PART B SECTION

OR

ANSWER 2 QUESTIONS FROM THIS PART A SECTION AND 3 QUESTIONS FROM THE PART B SECTION

Q1: For the circuit shown in Figure-1,

(a) Calculate the equivalent resistance of the circuit , R_{AB} at the terminals A and B. [10]

(b) When 50V dc source is switched at terminals A-B, solve for the voltage V_1 at the location shown. [10]

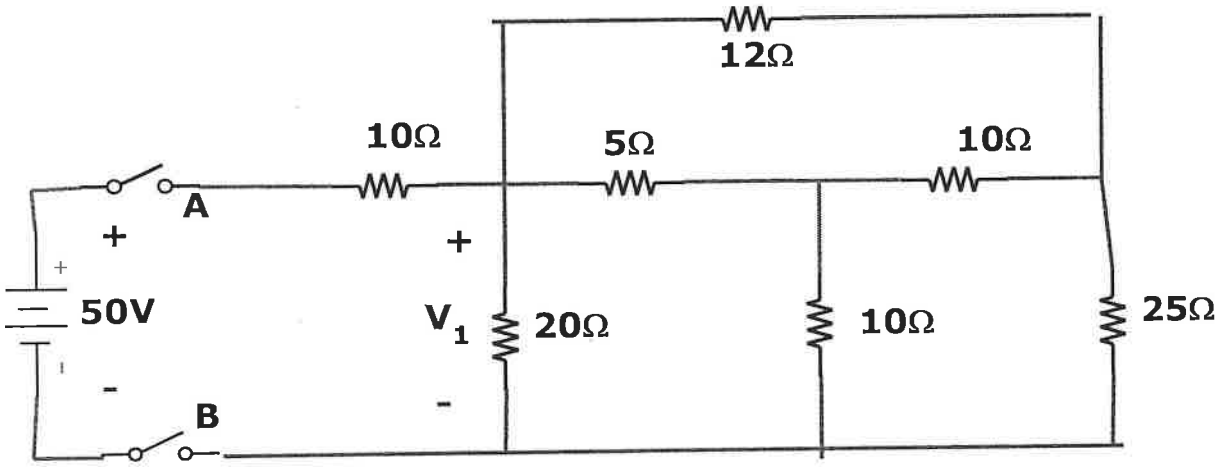


Figure-1

Q2: In the circuit shown in Figure-2,

(a) Write the node voltage equations for V_1 ,V_2 ,V_3 and V_4 . [10]

(b) Solve the node voltages. [10]

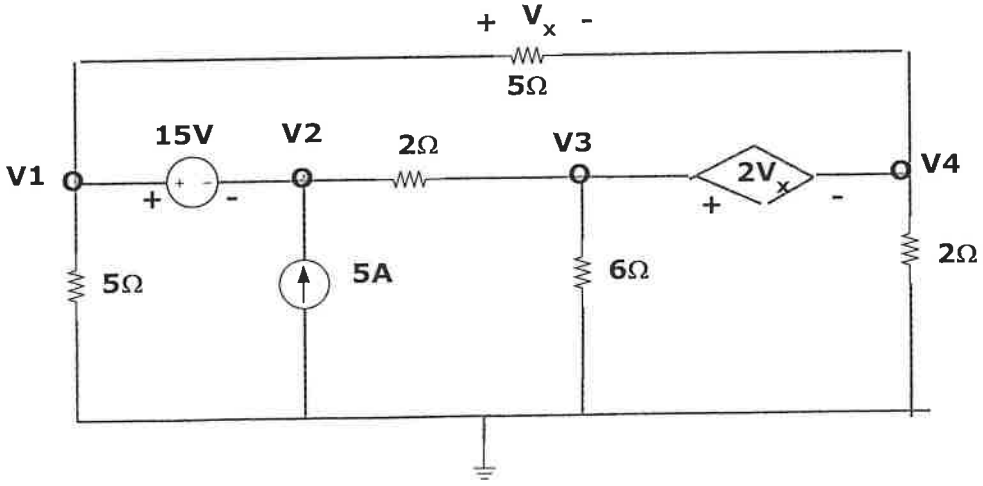


Figure-2

Q3: In Figure-3, the switch was initially closed for a long time. At t = 0, it is opened.

Calculate (i) $v_c(0+)$, $\frac{dv_c}{dt}(0+)$, $i_c(0+)$ and $v_c(\infty)$ [4+4+2+2]

(ii) $v_c(t)$ when $t \geq 0$ [8]

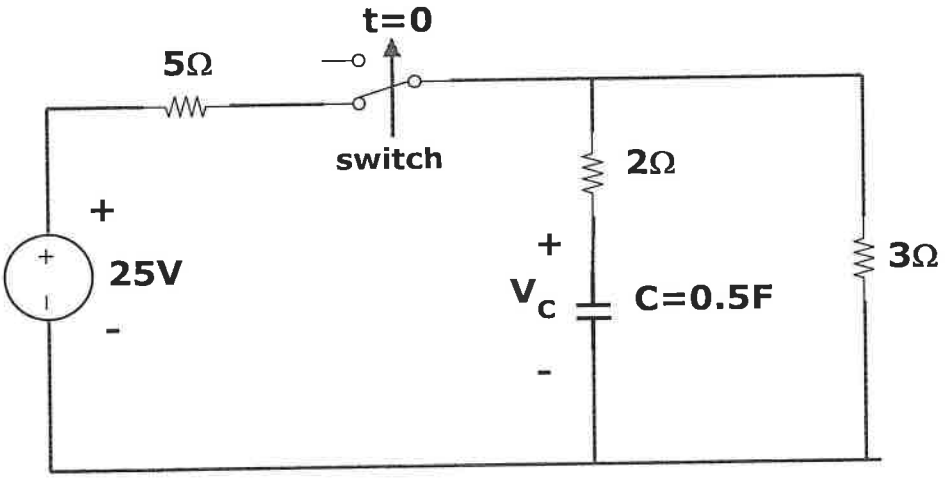


Figure-3

Q4: **(a)** Thevenize (find V_{th} and Z_{th}) at terminals A –B of the circuit shown in Figure-4. [6+6]

(c) Calculate Z_{load}, to be connected across the terminals A and B for maximum power dissipation in Z_{load}. [2]

(b) Calculate this P_{max}, maximum possible power dissipation in Z_{load}. [6]

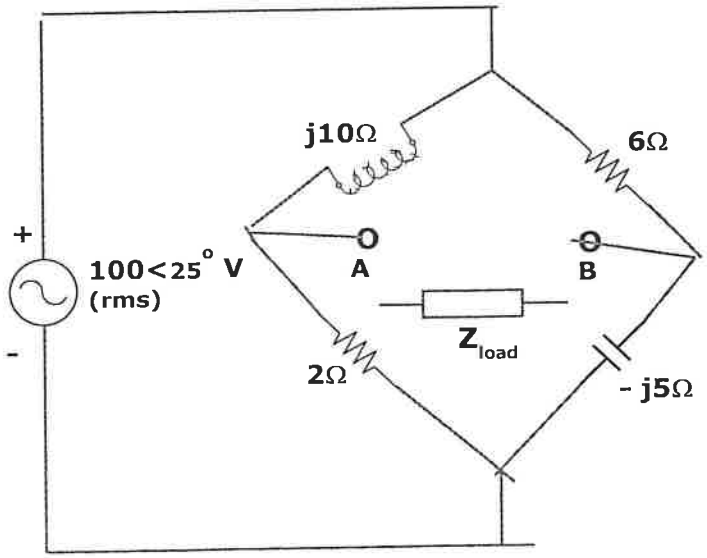


Figure-4

Q5: In Figure-5, solve the voltage across the capacitor, $V_o(t)$ by Superposition Theorem. [20]

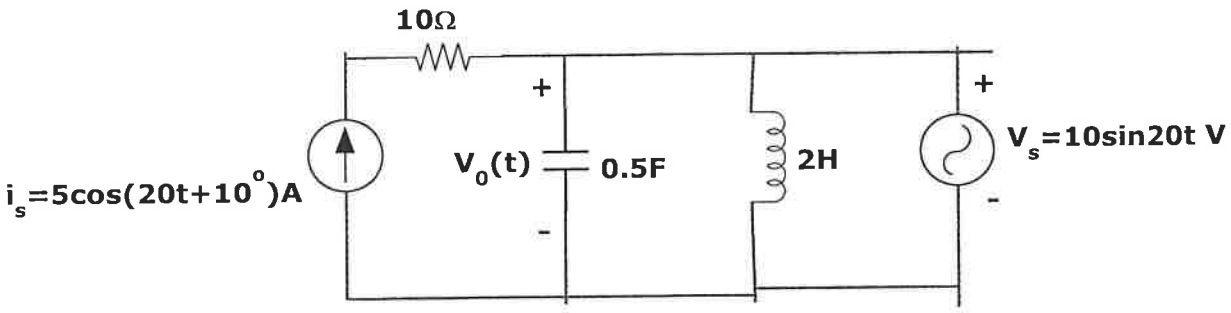


Figure-5

Q6: In the circuit shown in Figure-6, the switch was closed at t=0. Initial voltage at the capacitor and initial current in the inductor are shown in the diagram..

(a) Draw the Laplace Transformed circuit at $t \geq 0$. [10]

(c) Solve $V_c(t)$ by Laplace transform. [10]

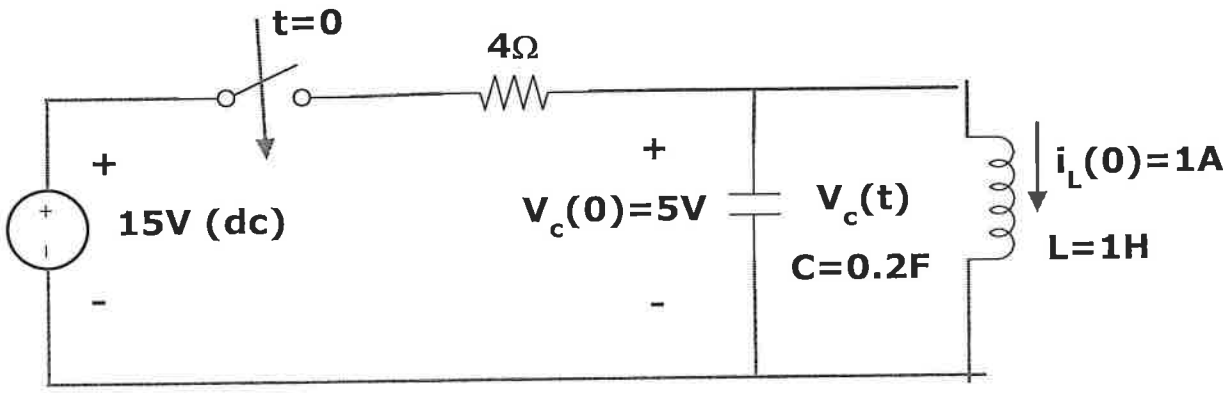


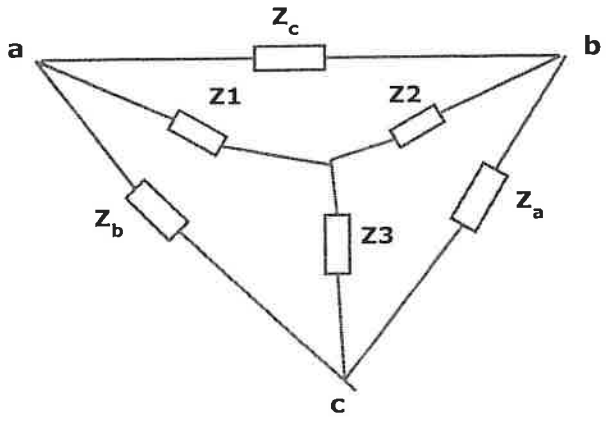
Figure-6

Appendix

Some useful **Laplace Transforms:**

f(t)	→	F(s)
Ku(t)		K /s
$\partial(t)$		1
t		$1/s^2$
e^{-at} u(t)		1 / (s+a)
sin wt .u(t)		$w / (s^2+w^2)$
cos wt . u(t)		$s / (s^2+w^2)$
$e^{-\alpha t} \sin \omega t$		$\frac{\omega}{(s+\alpha)^2+\omega^2}$
$e^{-\alpha t} \cos \omega t$		$\frac{(s+\alpha)}{(s+\alpha)^2+\omega^2}$
$\frac{df(t)}{dt}$		$s F(s) - f(0^-)$
$\frac{d^2 f(t)}{dt^2}$		$s^2F(s) - s f(0^-) - f^1(0^-)$
$\int_{-\infty}^{t} f(q)dq$		$\frac{F(s)}{s} + \int_{-\infty}^{0} f(q)dq$

Star – Delta conversion:



$$Z_1 = \frac{Z_b . Z_c}{Z_a + Z_b + Z_c} \qquad Z_2 = \frac{Z_a . Z_c}{Z_a + Z_b + Z_c} \qquad Z_3 = \frac{Z_a . Z_b}{Z_a + Z_b + Z_c}$$

$$Z_a = \frac{Z_1 . Z_2 + Z_2 . Z_3 + Z_3 . Z_1}{Z_1} \qquad Z_b = \frac{Z_1 . Z_2 + Z_2 . Z_3 + Z_3 . Z_1}{Z_2}$$

$$Z \quad = \frac{Z_1 . Z_2 + Z_2 . Z_3 + Z_3 . Z_1}{Z_3}$$

$$x(t) = x(\infty) + [x(0^+) - x(\infty)]e^{-\frac{t}{\tau}} \qquad \tau = R \cdot C \qquad \tau = \frac{L}{R}$$

$$Z = R + j(X_L - X_C) = \lfloor Z \rfloor \angle\theta, \quad \theta = tan^{-1}[\frac{(X_L - X_C)}{R}]$$

$$P = V.I\ cos\theta, \qquad Q = V.I\ sin\theta \qquad Power\ Factor = cos\theta$$

$$V_{rms} = \frac{V_m}{\sqrt{2}} \qquad Z_L = Z_{th}^* \qquad P_{max} = \frac{V_{th(rms)}^2}{4R_{th}} = \frac{V_{mth}^2}{8R_{th}}$$

16-MEX-A2

PART B

ELECTRONICS

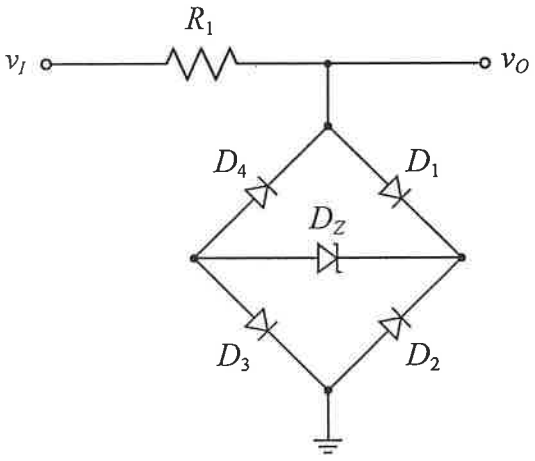
ANSWER A MAXIUM OF 3 QUESTIONS FROM THIS PART B SECTION AND TWO QUESTIONS FROM THE PART A SECTION

OR

ANSWER 2 QUESTIONS FROM THIS PART B SECTION AND 3 QUESTIONS FROM THE PART A SECTION

QUESTION (1)

Sketch accurately the transfer characteristic (v_O versus v_I) of the following circuit for an input voltage of ±20 V. Make sure to specify all the break points and slopes. (20 points)



Given:

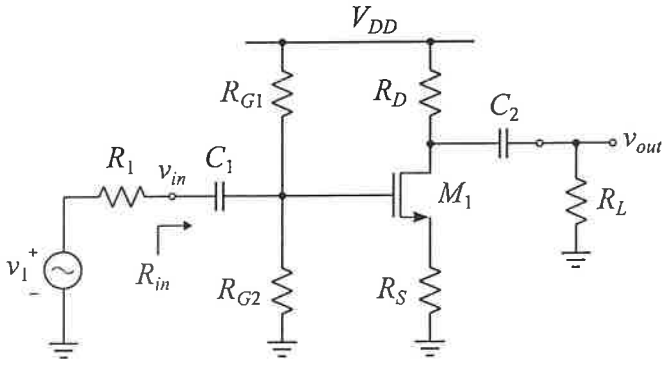
1) All diodes can be represented by a piece-wise linear model.
2) The *pn* junction diodes D_1 to D_4 have $V_{D0} = 0.65$ V and $r_D = 20\ \Omega$.
3) The zener diode D_Z, has $V_{Z0} = 8.2$ V and $r_z = 20\ \Omega$.
4) $R_1 = 1$ kΩ.

QUESTION (2)

The following is a single stage common source amplifier circuit.
Given: $V_{TH} = 1$V, $K = 4$ mA/V^2, and $\lambda = 0$

a) For a supply voltage $V_{DD} = 15$ V, design the bias circuit such that $I_D = 0.5$ mA, $V_S = 3.5$ V, and $V_D = 6$ V. Please specify the values for R_{G1}, R_{G2}, R_S and R_D. (10 points)

b) Assuming that the equivalent input resistance R_{in} = 1.67 MΩ, R_1 = 100 kΩ, R_L = 200 kΩ, determine the overall small signal voltage gain v_1/v_{out}. (10 points)



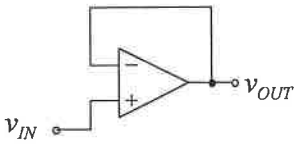
Useful formulae: for n-channel MOSFET

$$i_{DS} = K\left[(v_{GS} - V_{TH})v_{DS} - \frac{1}{2}v_{DS}^2\right] \qquad \text{triode region}$$

$$i_{DS} = \frac{1}{2}K(v_{GS} - V_{TH})^2(1 + \lambda v_{DS}) \qquad \text{saturation region}$$

QUESTION (3)

An op amp with a slew rate of 1 V/μs and a unity-gain bandwidth, f_t of 1 MHz is connected in the unity-gain follower configuration.



a) What is the largest possible input voltage step for which the output voltage waveform can still produce exponentially rising and falling waveforms? (8 points)

b) For this input voltage, find the 10% to 90% rise time. (6 points)

c) If the input step is 10 times larger than the voltage that you have found in part (a), find the new 10% to 90% rise time. (6 points)

Given:

Supply Voltage = ±10 V

Useful Formulae:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1+s/\omega_t}, \quad v_{OUT}(t) = V\left(1-e^{-\omega_t t}\right)$$

QUESTION (4)

In the following CMOS inverter, the threshold voltages of the *n*- and *p*-channel transistors are V_{Tn} and $-|V_{Tp}|$, respectively:

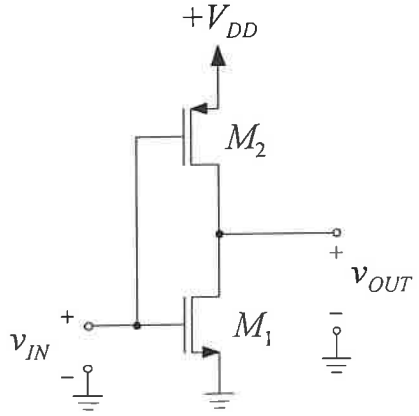
a) Draw the input to output voltage transfer characteristic (VTC) for this inverter. Express and label clearly all voltage levels on the VTC plot. (20 points)

b) Indicate the noise margins NM_L and NM_H on the VTC.

c) Indicate the logic high and low output voltage levels V_{OH}, V_{OL} on the VTC.

d) Indicate the logic high and low input voltage levels V_{IH}, V_{IL} on the VTC.

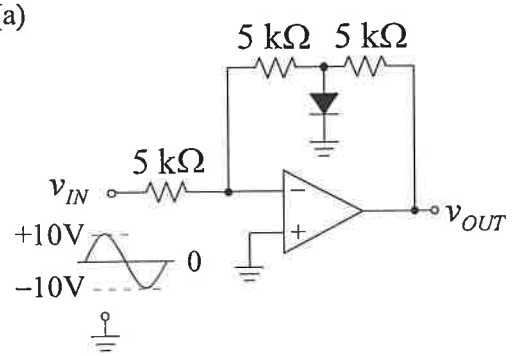
e) Indicate clearly the mode of operation in each region of the VTC.



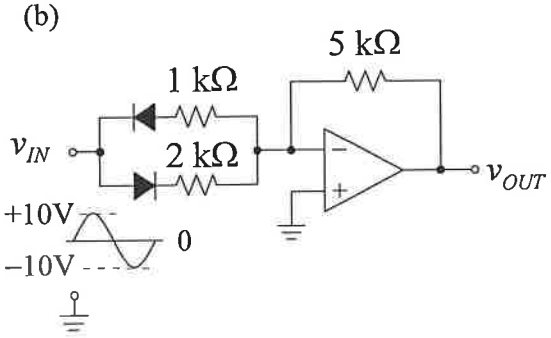
QUESTION (5)

In the following circuits, assume that the diode is ideal and has a forward voltage drop of 0.7V, and all op amps are ideal and with supply voltages of ±15 V. Sketch the output waveform for one complete sine wave input cycle. (20 points)

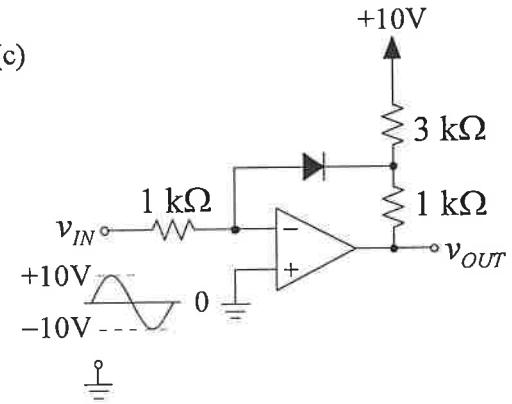
(a)



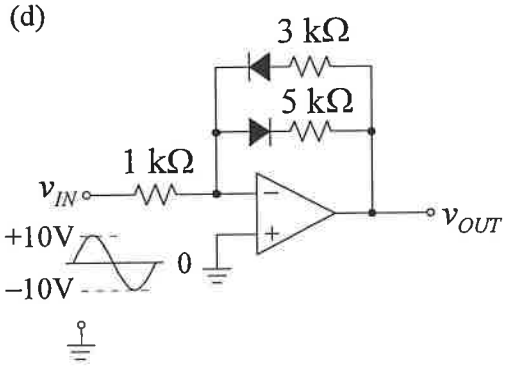
(b)



(c)



(d)



(e)