National Exams December 2018

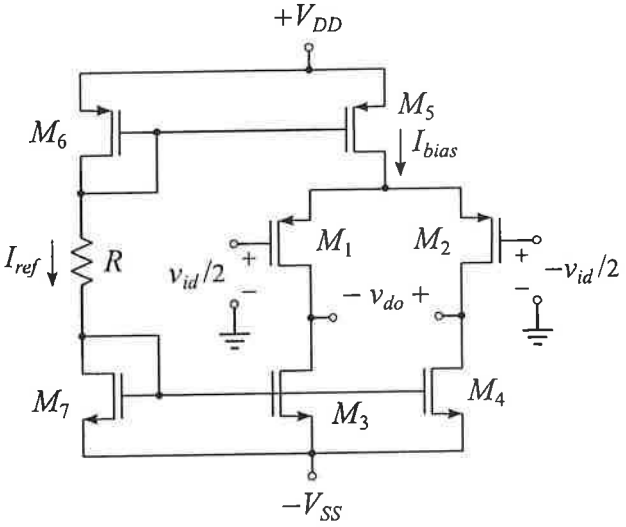
16-Elec-B5, Advanced Electronics

3 hours duration

Notes:

1. If any doubt exists as to the interpretation of any question, the candidate is urged to submit, within their answer, a clear statement of any assumptions made.
2. This is a **CLOSED BOOK EXAM**.
   Approved Casio or Sharp calculator is permitted.
3. Answer all **FIVE** (5) questions.
4. All questions are worth 20 marks each.
5. Please start each question on a new page and clearly identify the question number and part number, e.g. Q4(a).
6. In schematics, ground and chassis may be assumed to be common, unless specifically stated otherwise.
7. Unless otherwise specified, assume that Op-Amps are ideal and that supply voltages are ±15V.
8. If questions require an answer in essay format, clarity and organization of the answer are important. Provide block diagrams and circuit schematics whenever necessary.

QUESTION (1) Design this CMOS amplifier to have the following characteristics:



a) Differential gain $A_d = v_{do}/v_{id} = 50$ V/V

b) $I_{ref} = I_{bias} = 200$ µA

c) The DC gate voltages, $V_{G5} = V_{G6} = 0.8$ V

d) The DC gate voltages, $V_{G3} = V_{G4} = V_{G7} = -0.8$ V

Given: $V_{DD} = |V_{SS}| = 1.5$ V, $|V_{TH}| = 0.5$ V, $\mu_n C_{ox} = 2.5\mu_p C_{ox} = 250$ µA/V^2, and $\lambda = 0.1$

channel length modulation can be neglected in all DC bias calculations

Please provide the value for R and the W/L ratios, $|I_{DS}|$ and $|V_{GS}|$ for all transistors. (20 points)

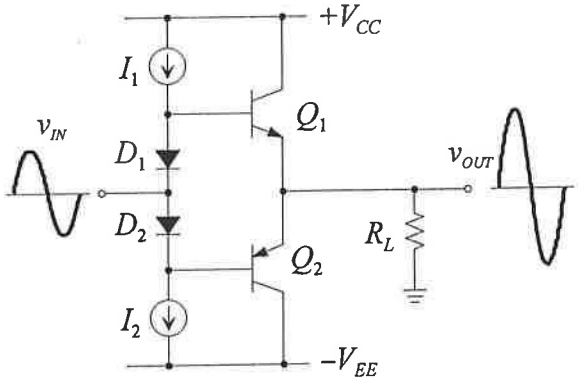
QUESTION (2)

In the following push-pull output stage, assume that each transistors conducts a negligible amount of current around $v_{IN} = 0$V. Q_1 conducts for the positive half of the input voltage and Q_2 conducts for the negative half. Assuming that $V_{CC} = |V_{EE}| = 10$V, $R_L = 8\Omega$, and the input voltage is sinusoidal, determine the followings:

a) The maximum rms power that can be delivered to the load, R_L. (5 points)

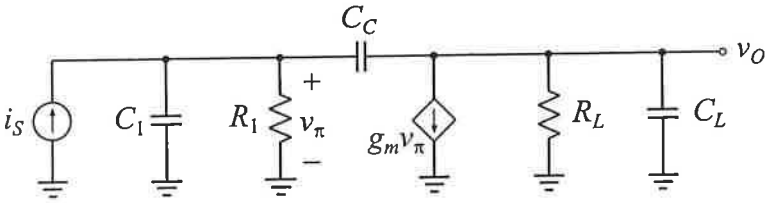
b) The rms power dissipated by transistor Q_1 when delivering maximum rms power to the load. Assume that the base current is negligible. (10 points)

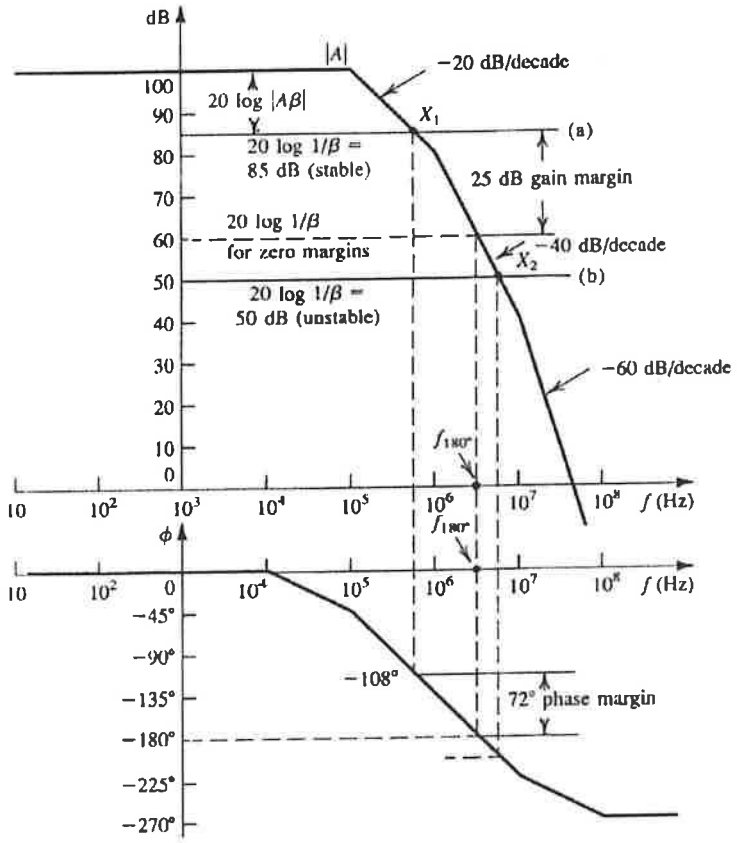
c) The maximum power efficiency of this push-pull stage? Neglect the power drawn by the bias current sources I_1 and I_2. (5 points)



QUESTION (3)

An op amp has an open-loop transfer function (without C_C) and the corresponding equivalent circuit as shown below. The open-loop first pole and second pole locations are at 0.1 MHz and 1 MHz, respectively. The first pole is caused by the input circuit of that stage, and that the second pole is introduced by the output circuit. Compensate this op amp using C_C such that it will be stable. Provide justification for your choice of C_C. What will be the frequencies of the new first and second poles? What will be the new phase margin? (20 points)





Source: Sedra and Smith, Microelectronics

Given:

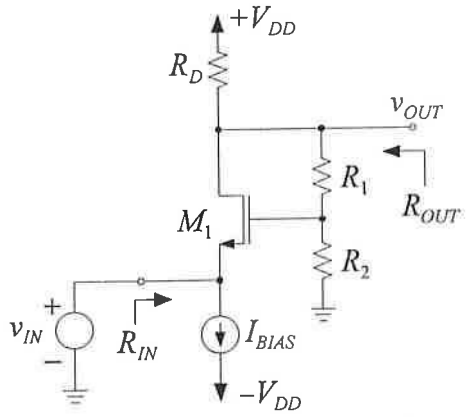
$C_1 = 100$ pF

$C_L = 5$ pF

$g_m = 40$m A/V

QUESTION (4)

In the following amplifier can be considered as a feedback circuit. You can assume that the transistor is operating in saturation mode.



a) Determine the input and output resistance (R_{IN} and R_{OUT}) if there is no feedback network (i.e. $R_1 = \infty$, and $R_2 = 0\ \Omega$).
(8 points)

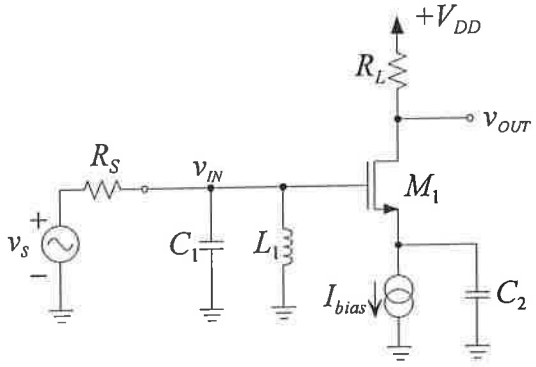
b) Derive the input and output resistance (R_{IN} and R_{OUT}) if the feedback network has finite values for R_1 and R_2.
(12 points)

Express you answer in terms of g_m, R_D, R_1 and R_2.

The following single stage differential amplifier circuit is designed for a 0.18 μm CMOS technology.

QUESTION (5)

In the following tuned amplifier circuit, the transistor parameters are given as $K = 1$ mA/V^2, $V_{TH} = 1$ V, $C_{gs} = 10$ pF, $C_{gd} = 1$ pF, and $\lambda = 0$.



For: $L_1 = 1$ μH
$C_1 = 200$ pF, $C_2 = \infty$
$R_S = 1$ kΩ, $R_L = 2$ kΩ
$I_{bias} = 2$ mA
$V_{DD} = 10$ V

a) What is the center frequency, ω_o of this amplifier? (4 points)

b) What is the gain v_{OUT}/v_S at $\omega = \omega_o$? (8 points)

c) What is the 3dB bandwidth of this tuned amplifier? (8 points)