National Exams May 2019

16-Elec-A4, Digital Systems and Computers

3 hours duration

NOTES:

1. If doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumptions made.

2. This is a Closed Book exam.
   Candidates may use one of two calculators, the Casio or Sharp approved models.

3. FIVE (5) questions constitute a complete exam.
   Clearly indicate your choice of any five of the six questions given otherwise the first five answers found will be considered your pick.

4. All questions are worth 12 points.
   See below for a detailed breakdown of the marking.

Marking Scheme

1. (a) 3, (b) 3, (c) 3, (d) 3, total = 12
2. (a) 3, (b) 3, (c) 3, (d) 3, total = 12
3. (a) 6, (b) 6, total = 12
4. (a) 3, (b) 4, (c) 3, (d) 2, total = 12
5. (a) 3, (b) 3, (c) 3, (d) 3, total = 12
6. (a) 4.5, (b) 4.5, (c) 3, total = 12

The number beside each part above indicates the points that part is worth

1.- Given the following function in product-of-sums (PoS) form:

$$f(A,B,C,D) = \prod M_i(0,2,6,7,8,10,14,15)$$

Map the function f in a K-map and:

(a) Find the minimized PoS expression for *f*.

(b) Check if the minimized expression found in (a) is hazard-free. Justify.

If it is not hazard-free provide the smallest PoS hazard-free expression for *f*.

(c) Find the minimized sum-of-products (SoP) expression for *f*.

(d) Check if the minimized expression found in (c) is hazard-free. Justify.

If it is not hazard-free provide the smallest SoP hazard-free expression for *f*.

2.- Design a sequential circuit with two JK flip-flops, A and B, and two inputs E and X that performs as follows:

- If E = 0 the circuit remains in the same state regardless the value of X,
- When E = 1 and X = 1 the circuit goes through the state transitions AB = 00 to 01 to 10 to 11 back to 00, and repeats,
- When E = 1 and X = 0 the circuit goes through the state transitions AB = 00 to 11 to 10 to 01 back to 00, and repeats.

Provide:

(a) the state transition diagram,

(b) the state transition table,

(c) the K-map simplification of the combinational logic required, as well as

(d) a drawing of the resulting logic circuit diagram.

Note: Consult flip-flop excitation tables attached at the end as needed.

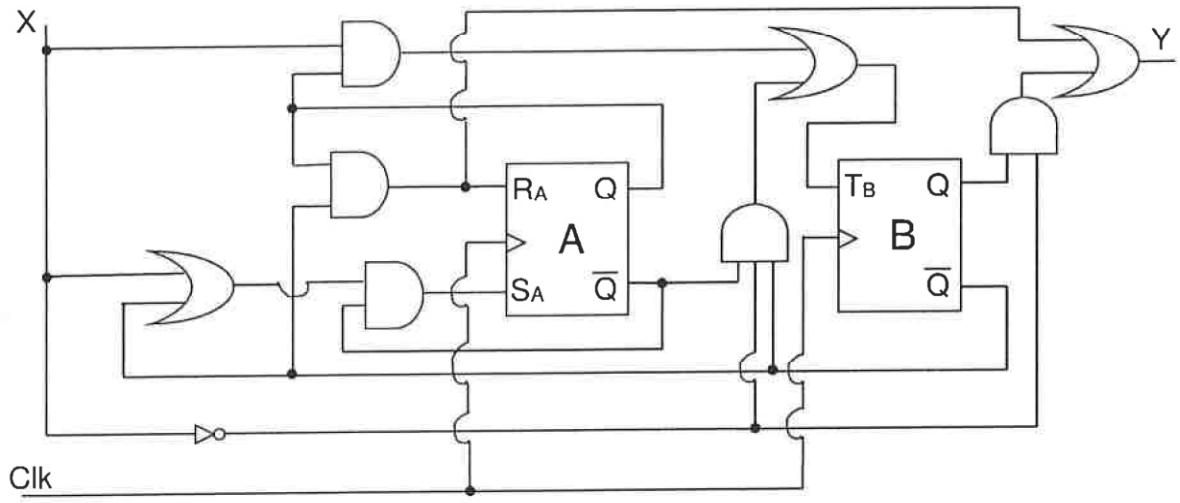
3.- The following is a truth table of a 3-input, 4-output combinational circuit.

(a) Use K-maps to obtain the simplified expressions for A, B, C and D.

(b) Implement them using a Programmable Logic Array (PLA) architecture.

Inputs			Outputs			
A	B	C	X	Y	Z	W
0	0	0	0	1	1	1
0	0	1	0	1	1	1
0	1	0	1	0	0	1
0	1	1	0	1	0	1
1	0	0	0	0	0	0
1	0	1	0	1	1	1
1	1	0	1	1	0	1
1	1	1	1	1	0	0

4.- The following circuit with input X and output Y uses one RS flip-flop and a T flip-flop.



(a) Write the logic expressions for R_A, S_A, T_B and Y.

(b) Obtain the state transition table for the circuit.
Include A, B, X, R_A, S_A, T_B, A^+, B^+, Y in this order.

(c) Sketch the state transition diagram for the circuit.

(d) Is this a Moore or a Mealy machine? Explain.

Note: Consult flip-flop excitation table attached at the end as needed.

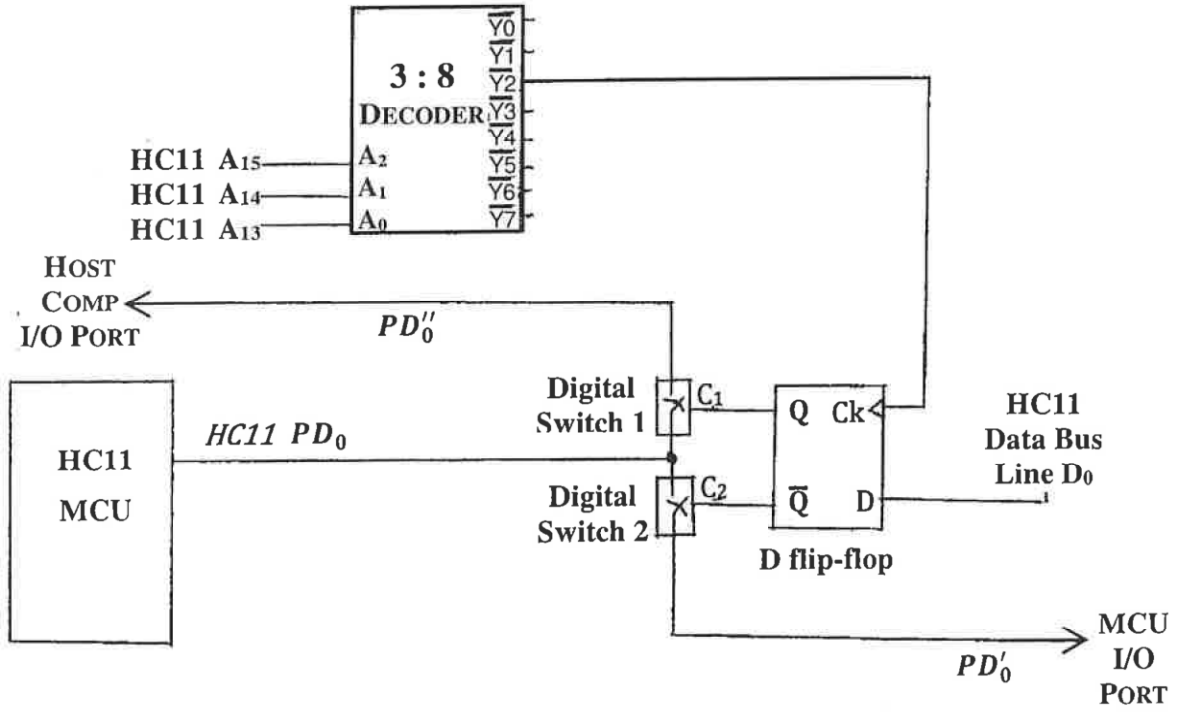
5.- The diagram below shows the use a D flip-flop governing two digital switches in order to route line PD_0 of the HC11 microcontroller unit (MCU) to one of two connectors: the HOST computer I/O port or the MCU I/O port connector.
Digitals switches close when control input C is at a logic '1' and remain open when C is '0'.
HC11 address lines A_{15} - A_{13} are connected to the 3 address inputs of a 3:8 decoder as shown in the figure, the most significant address input of the decoder is A_2 and the least significant is A_0. Assume the decoder is enabled and towards the end of the execution of each instruction cycle all its active-low outputs $\overline{Y}_0$ - $\overline{Y}_7$ go back to their inactive logic '1' state.
The least significant data bus line of the HC11 (D_0) is connected to the flip-flop D input.
Knowing that instruction
ldaa #$xx means load HC11 CPU register accumulator A with hexadecimal value **xx**, and
staa $zzzz means store the value in accumulator A to address **$zzzz,**
which of the following set of instructions will direct HC11 line PD_0 to the HOST computer I/O port, which to the MCU I/O port connector and which will not affect the current routing.
Mark your choice with an **X** and justify your selection in each case.

(a) ldaa #$10, staa $8000 [ ] HOST Comp I/O port, [ ] MCU I/O port, [ ] No Action

(b) ldaa #$29, staa $4000 [ ] HOST Comp I/O port, [ ] MCU I/O port, [ ] No Action

(c) ldaa #$B4, staa $5000 [ ] HOST Comp I/O port, [ ] MCU I/O port, [ ] No Action

(d) ldaa #$05, staa $2500 [ ] HOST Comp I/O port, [ ] MCU I/O port, [ ] No Action



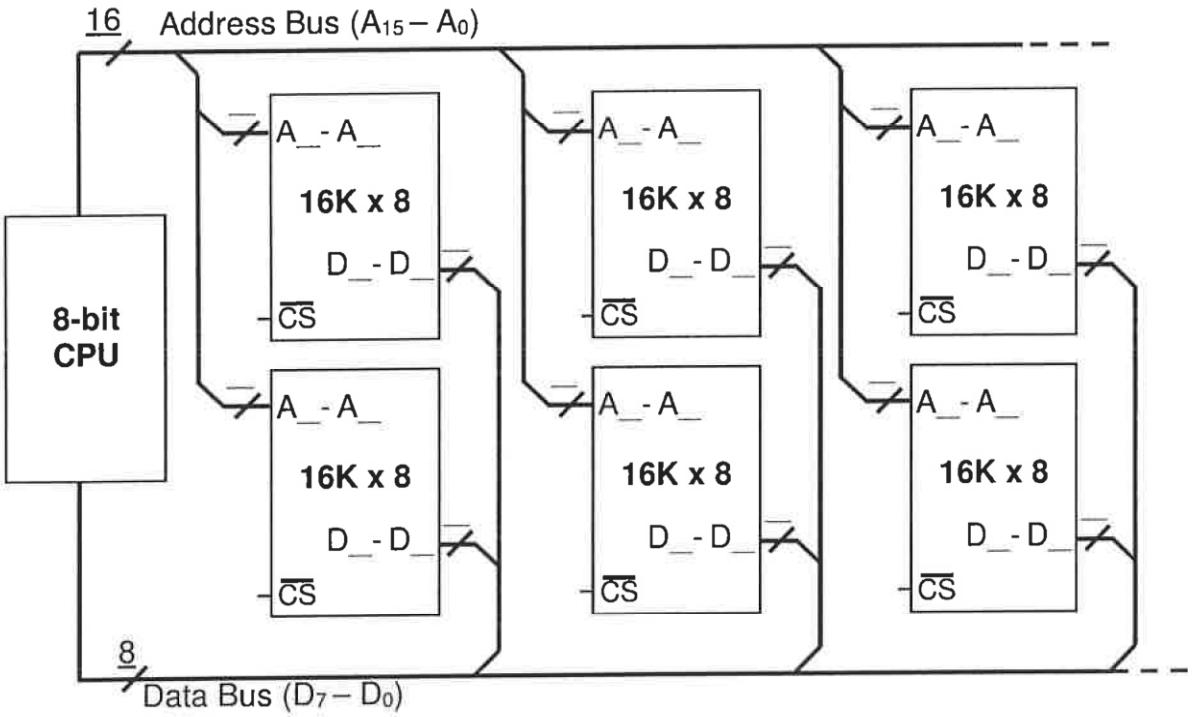
6.- Provide this 8-bit CPU with a 64Kbyte memory space by making use of 16K x 4 memory modules like the ones provided in the figure below.

(a) Fill in the blanks *beside* and *inside* the memory module with the appropriate numbers. The number on top of this symbol —/— represents the number of lines on that bus. The spaces besides the A's and the D's are to indicate which lines of the address and data busses are connected to each module, respectively.

(b) Complete the connections in the figure below adding logic gates where needed to produce the chip select ($\overline{CS}$) signals needed in the decoding logic. Explain the reasons for the connections made, include expressions for the Boolean logic used.

(c) Provide the address range allocated to each of the modules used.

Note: R/$\overline{W}$ & clock signals are omitted for simplicity.



Excitation Table

Q	Q+	R	S	J	K	T	D
0	0	X	0	0	X	0	0
0	1	0	1	1	X	1	1
1	0	1	0	X	1	1	0
1	1	0	X	X	0	0	1

Basic Boolean Identities

	Identity	Comments
1.	$A+0=A$	Operations with 0 and 1
2.	$A+1=1$	Operations with 0 and 1
3.	$A+A=A$	Idompotent
4.	$A+\overline{A}=1$	Complementarity
5.	$A\cdot 0=0$	Operations with 0 and 1
6.	$A\cdot 1=A$	Operations with 0 and 1
7.	$A\cdot A=A$	Idompotent
8.	$A\cdot \overline{A}=0$	Complementarity
9.	$\overline{\overline{A}}=A$	Involution
10.	$A+B=B+A$	Commutative
11.	$A\cdot B=B\cdot A$	Commutative
12.	$A+(B+C)=(A+B)+C=A+B+C$	Associative
13.	$A\cdot(B\cdot C)=(A\cdot B)\cdot C=A\cdot B\cdot C$	Associative
14.	$A\cdot(B+C)=(A\cdot B)+(A\cdot C)$	Distributive
15.	$A+(B\cdot C)=(A+B)\cdot(A+C)$	Distributive
16.	$A+(A\cdot B)=A$	Absorption
17.	$A\cdot(A+B)=A$	Absorption
18.	$(A\cdot B)+(\overline{A}\cdot C)+(B\cdot C)=(A\cdot B)+(\overline{A}\cdot C)$	Consensus
19.	$\overline{A+B+C+\ldots}=\overline{A}\cdot\overline{B}\cdot\overline{C}\cdot\ldots$	De Morgan
20.	$\overline{A\cdot B\cdot C\cdot\ldots}=\overline{A}+\overline{B}+\overline{C}+\ldots$	De Morgan
21.	$(A+\overline{B})\cdot B=A\cdot B$	Simplification
22.	$(A\cdot\overline{B})+B=A+B$	Simplification