National Exams December 2016

07-Elec-B5, Advanced Electronics

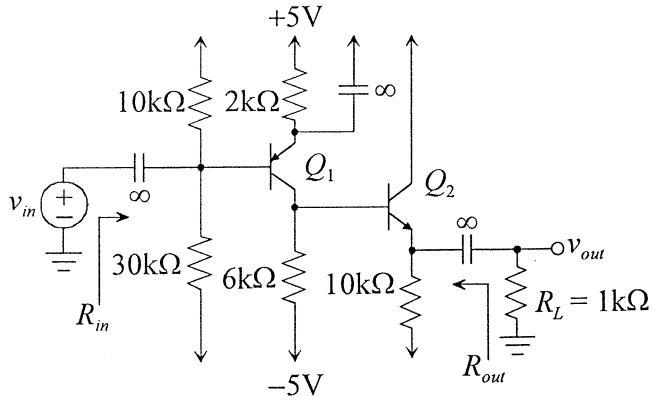
3 hours duration

Notes:

1. If any doubt exists as to the interpretation of any question, the candidate is urged to submit, within their answer, a clear statement of any assumptions made.
2. This is a **CLOSED BOOK EXAM**.
   Any non-communicating calculator is permitted.
3. Answer all **FIVE** (5) questions.
4. All questions are worth 20 marks each.
5. Please start each question on a new page and clearly identify the question number and part number, e.g. Q4(a).
6. In schematics, ground and chassis may be assumed to be common, unless specifically stated otherwise.
7. Unless otherwise specified, assume that Op-Amps are ideal and that supply voltages are ±15V.
8. If questions require an answer in essay format, clarity and organization of the answer are important. Provide block diagrams and circuit schematics whenever necessary.

QUESTION (1)

Assume $\beta = 100$, $|V_A| = \infty$, $|V_{BE(\text{on})}| = 0.7\text{V}$, and $|V_{CE(\text{sat})}| = 0.3\text{V}$



a) Determine the dc bias points: I_{C1}, I_{C2}, V_{E1}, V_{E2}, V_{C1}, and V_{B1}.

b) What is the gain v_{out}/v_{in} ?

c) What is R_{in}?

d) What is R_{out}?

(20 points)

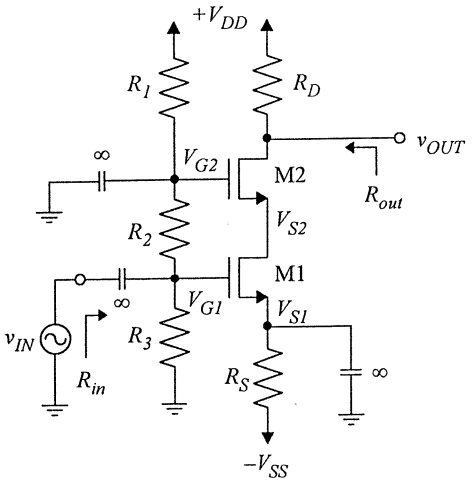
QUESTION (2)

Given: $V_{TH} = 1.2\text{V}$, $K = 0.8\text{mA/V}^2$, $\lambda = 0$,
$V_{DD} = V_{SS} = 5\text{V}$, and $R_L = 2\text{k}\Omega$

(a) Design the biasing circuit such that $I_{DS1} = 0.4\text{mA}$, $V_{DS1} = V_{DS2} = 2.5\text{V}$. Given that $R_S = 10\text{k}\Omega$, $R_1 + R_2 + R_3 = 300\text{k}\Omega$.

(b) What are the small signal voltage gain, v_{out}/v_{in}, the input and output resistance?

(20 points)



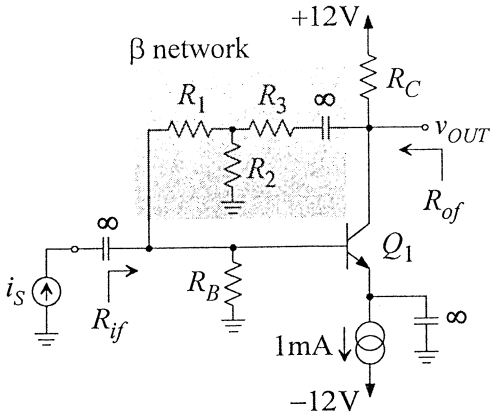
Useful formulae: for n-channel MOSFET

$$i_{DS} = K\left[(v_{GS} - V_{TH})v_{DS} - \frac{1}{2}v_{DS}^2\right] \qquad \text{triode region}$$

$$i_{DS} = \frac{1}{2}K(v_{GS} - V_{TH})^2(1 + \lambda v_{DS}) \qquad \text{saturation region}$$

QUESTION (3)

The following circuit can be considered as a CE amplifier with a β feedback network. Assuming that Q_1 has an infinite current gain ($\beta_1 = \infty$, not to be confused with the feedback ratio) and $r_o = \infty$.



Given:

$R_1 = R_2 = R_3 = 10\text{k}\Omega$, $R_B = R_C = 5\text{k}\Omega$, $V_T = 25\text{mV}$

a) Find the closed loop trans-resistance gain v_{OUT}/i_S in (V/A)

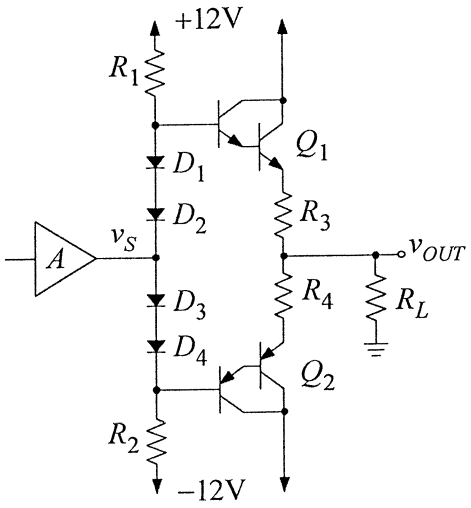
b) Find the input resistance, R_{if} seen by the input current source i_S.

c) Find the output resistance, R_{of} at the output terminal.

(20 points)

QUESTION (4)

The following class AB amplifier stage is biased such that the dc output voltage is 0V if the input voltage, v_S is zero. The forward voltage drop of the diodes D_1 to D_4 are 0.7V (independent of current level) and $|V_{BE}|$ for the complementary power Darlington transistors Q_1 and Q_2 are 1.2V (independent of current level). The input voltage, v_S is supplied by an ideal voltage amplifier, A which can be considered to be consuming zero power.



(20 points)

Given:

$\beta = 500$, and $|V_{CE(sat)}| = 0.3\text{V}$ for Q_1 and Q_2

$R_1 = R_2 = 1\text{k}\Omega$, $R_3 = R_4 = 5\Omega$, $R_L = 8\Omega$

a) Estimate the standby power, $P_{standby}$ with $v_S = 0\text{V}$.

b) Find the maximum peak to peak output voltage swing, $V_{O(p\text{-}p)}$. Hint: remember to take R_3 and R_4 into account.

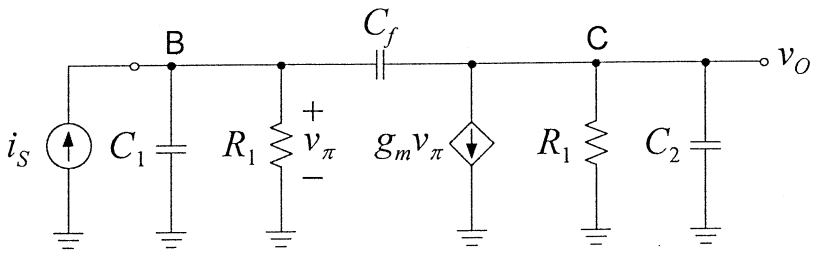
c) What is the minimum input voltage level for v_S to achieve maximum peak output?

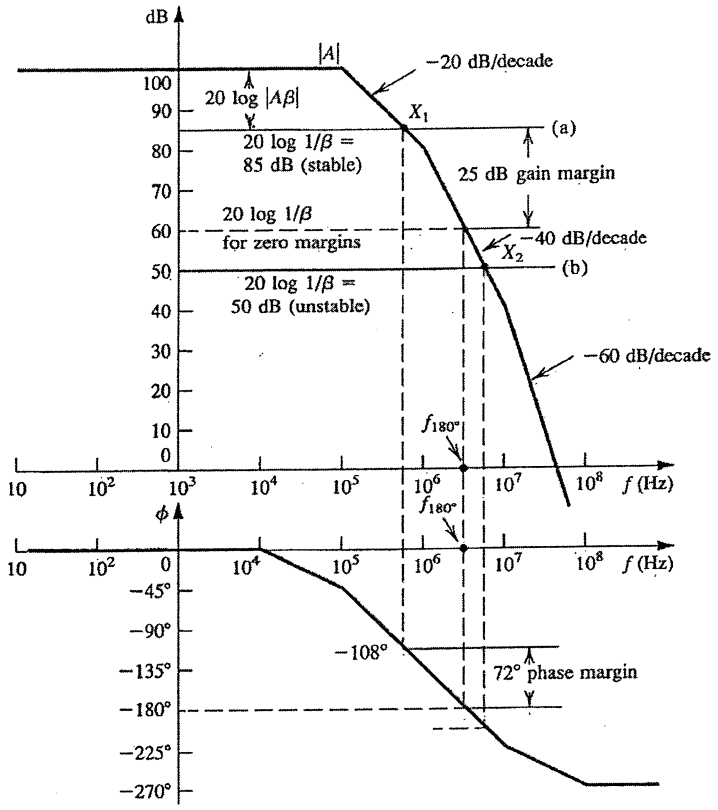
d) Find the maximum *rms* output power, $P_{out(max)}$ that can be delivered to R_L.

e) Find the efficiency, η of this output stage when delivering maximum output power.

QUESTION (5)

An op amp has an open-loop transfer function (without C_f) and the corresponding equivalent circuit as shown below. The open-loop first pole and second pole locations are at 0.1 MHz and 1 MHz, respectively. The first pole is caused by the input circuit of that stage, and that the second pole is introduced by the output circuit. Compensate this op amp using C_f such that it will be stable. Provide justification for your choice of C_f. What will be the frequencies of the new first and second poles? What will be the new phase margin? (20 points)





Given:

$C_1 = 100$ pF

$C_2 = 5$ pF

$g_m = 40$m A/V

Source: Sedra and Smith, Microelectronics