National Exams December 2018

04-BS-8, Digital Logic Circuits

3 hours duration

NOTES:

1. If a doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumption made with the answer of the question.

2. Candidates may use one of two calculators, the Casio or Sharp approved models. This is a closed book examination; however, candidates are allowed to bring one hand-written information sheet (8.5" X 11") of self-prepared notes.

3. This paper contains **FIVE (5)** questions and comprises **six (6)** pages.

4. Any **FOUR (4)** questions constitute a complete paper. Only the first four questions as they appear in your answer book will be marked.

5. All questions are of equal marks. Total marks = 100.

6. Each question carries 25 marks and the marks for each part of the questions are indicated in brackets.

7. A PAL16R4 Data sheet is provided in the Appendix. It can be used to provide the solution of Question 4, part (c) and should be attached to your answer sheet.

1. Design a synchronous up-down counter that has the following up and down sequences: (0, 1, 2, 3, 4, 5, 6, 7 & repeat) and (0, 7, 6, 5, 4, 3, 2, 1 & repeat). The counter has a 1-bit control input (UD), such that the counter counts upward for UD = 0 and counts downward when UD =1. Use negative edge triggered D-type flip-flops and logic gates to implement the up-down counter design.

(a) Start your design with a state table.

(5 marks)

(b) Develop the next state equations and simplify them if required. Show your complete work.

(13 marks)

(c) Implement and draw the synchronous counter circuit.

(7 marks)

2. (a) Construct a JK flip-flop by using a SR flip-flop and minimum number of logic gates. Draw a complete diagram of the JK flip-flop.

(6 marks)

(b) There are two types of sequential machines: Moore and Mealy type. Generally, which type of machine is prone to noise at its inputs? Justify your answer.

(5 marks)

(b) Contrast the similarities and differences between 2's complement and sign magnitude representations of binary numbers along with highlighting the advantages and disadvantages of each representation.

(6 marks)

(c) Which of the following binary values is closest to the decimal value $(1.03)_{10}$. Justify your answer

i. $(1.01)_2$ ii. $(1.0001)_2$

iii. $(1.00001001)_2$ iv. $(1.0101001)_2$

(8 marks)

3. Design and draw a combinational logic circuit to convert a 4-bit negative binary number $(A_3A_2A_1A_0)_2$ into 2's complement number as shown in Figure Q3. Assume that the input $(A_3A_2A_1A_0)_2$ is the magnitude of the negative input number.

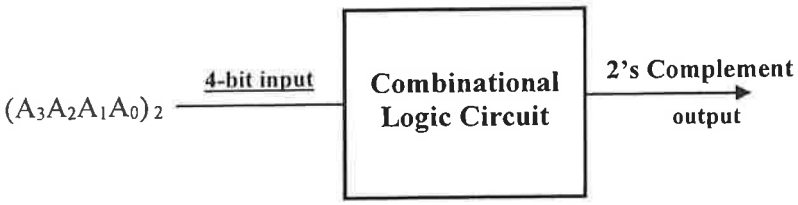


Figure Q3

The converted 2's complement number should be instantly available at the output.

(a) Construct the truth table of the circuit indicating the input and outputs.

(7 marks)

(b) Simplify the output Boolean functions by using K-maps and write the reduced Boolean functions of each output.

(12 marks)

(c) Implement the combinational logic circuit developed in part (b) by using minimum number of gates.

(6 marks)

4. A digital system that can detect a sequence of bits at its serial input channel is required. The sequence detector receives a serial data stream and a synchronizing clock from a data system as shown in Figure Q4. The sequence detector circuit asserts its output (**det**) for one clock cycle whenever it receives a binary sequence of **1110** followed by any number of 1's. The main features of the system are given below:

- Clock signal from the data system unit shifts the data bits out.
- Each input bit spans between consecutive negative transitions of the clock.
- The sequence always starts with the least significant bit.

Question No. 4 continues on Page 4

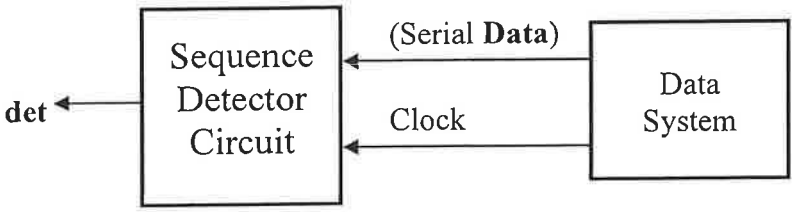


Figure Q4

Design the sequence detector such that its output, **det** goes to logic high during the 4th bit of a valid sequence.

(a) Draw the state diagram and state table for the sequence detector sequential circuit.

(7 marks)

(b) Design the sequence detector by using suitable edge-triggered (negative or positive) D-type flip-flops.

(10 marks)

(c) Implement the sequence detector designed in part (b) by using a PAL16R4 device. The logic diagram of PAL16R4 is given in the Appendix. Show the intact PAL fuses by crossing them in the diagram and attach it to your answer book.

(8 marks)

5. Braille is a system of raised dots that can be read by a blind person. Modified Braille patterns for 4-bit Hex numbers 0-F are shown in Figure Q5.

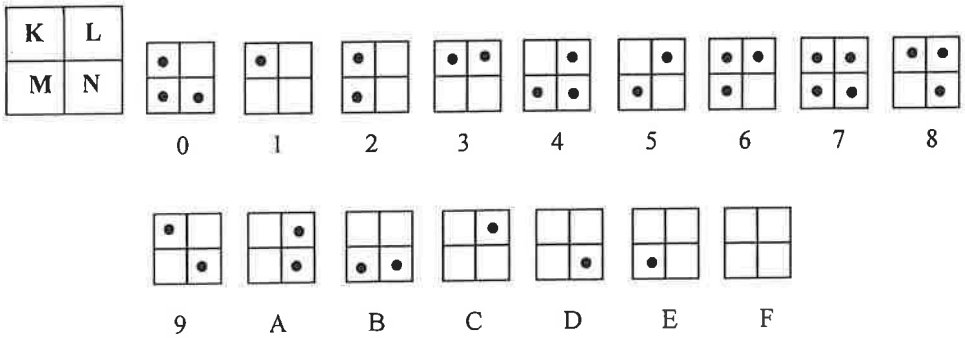


Figure Q5

Question No. 5 continues on Page 5

(a) Design a digital system that converts the 4-bit Hex numbers to Braille. Derive the minimized Boolean equation for each of the four Braille dot outputs (K, L, M, N) given a 4-bit Hex number ($X_3X_2X_1X_0$) as input. The 4-bit Hex inputs and the Braille dot outputs are all active-HIGH.

(16 marks)

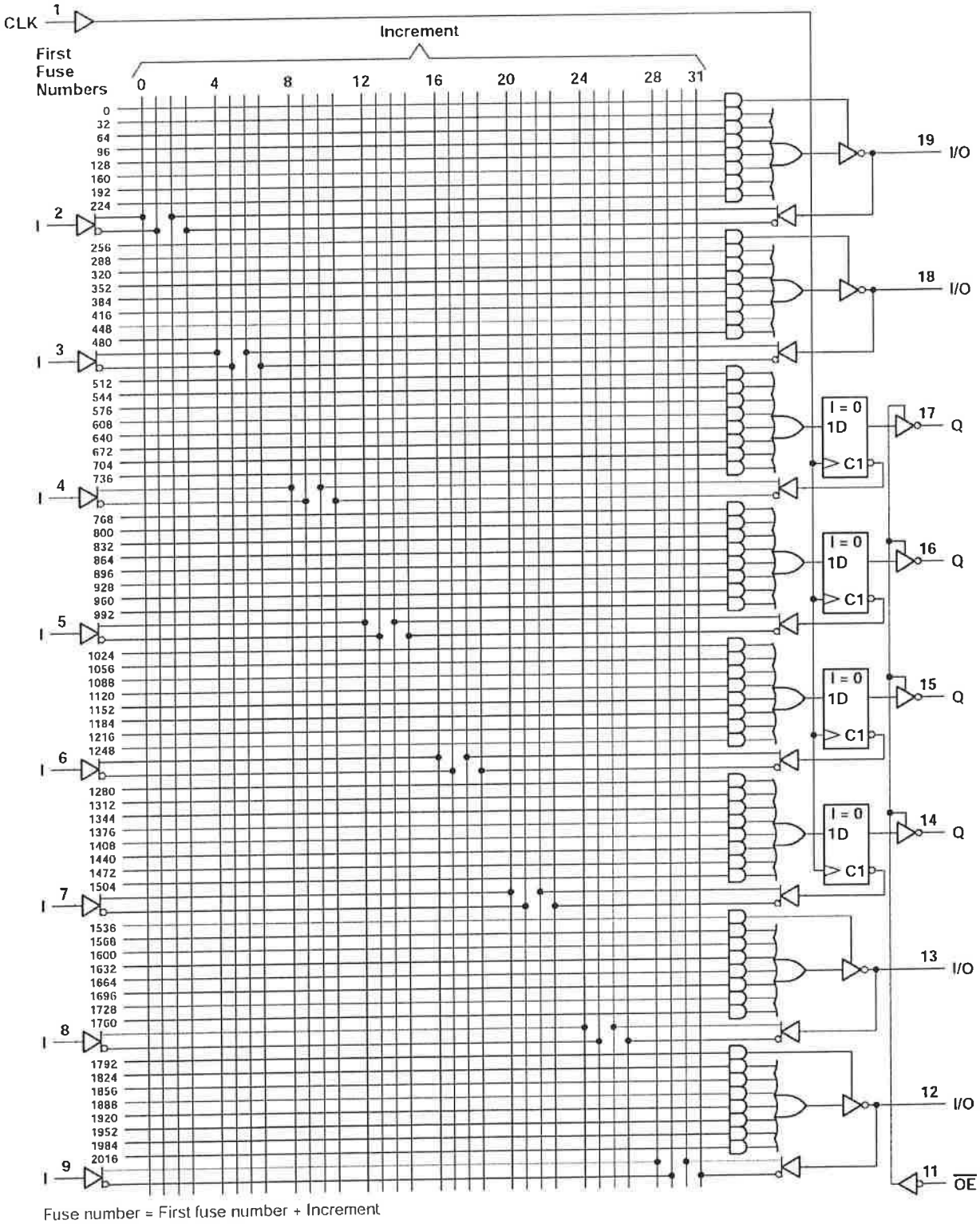
(b) Implement the minimized Boolean equation for outputs, K and M by using only 2-input NAND gates.

(9 marks)

End of Questions

APPENDIX

PAL16R4



Fuse number = First fuse number + Increment

End of Paper