National Exams May 2015

04-BS-8, Digital Logic Circuits

3 hours duration

NOTES:

1. If a doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumption made with the answer of the question.

2. Candidates may use one of two calculators, the Casio or Sharp approved models. This is a closed book examination; however, candidates are allowed to bring one hand-written information sheet (8.5" X 11") of self-prepared notes.

3. This paper contains **FIVE (5)** questions and comprises **SIX (6)** pages.

4. Any **FOUR (4)** questions constitute a complete paper. Only the first four questions as they appear in your answer book will be marked.

5. All questions are of equal marks. Total marks = 100

6. Each question carries 25 marks and the marks for each part of questions are indicated in brackets.

7. A PAL16L8 Data sheet is provided in the Appendix. It can be used to provide the solution of Question 2, part (b) and should be attached to your answer sheet.

1. A digital system is to be developed that can detect a sequence of bits at its single-bit input serial channel. The sequence detector receives data stream bits (**DS**) in a serial way. A synchronizing clock that shifts the data-bits is also available along with the data stream bits. Each **DS** bit spans between consecutive positive transitions of the clock. Design the sequence detector as a sequential circuit such that its output, **out** goes to logic **HIGH** during the 5th bit of a valid sequence, **11010**. The sequence always starts with the most significant bit.

   (a) Draw the state diagram and state table for the sequence detector sequential circuit.

   (12 marks)

   (b) Design the sequence detector by using suitable edge-triggered (negative or positive) JK flip-flops.

   (13 marks)

2. (a) Identify the main differences between ROM and FPGA devices that are used to implement digital logic circuits.

   (6 marks)

   (b) Implement the following four Boolean expressions by using a PAL16L8 programmable logic device.

   F1(w, x, y, z) = $\sum$**m**(0, 2, 4, 6, 7, 9, 11, 13)
   F2(w, x, y, z) = $\sum$**m**(0, 1, 4, 6, 8, 10, 14)
   F3(w, x, y, z) = $\sum$**m**(1, 3, 4, 7, 9, 12, 15)
   F4(w, x, y, z) = $\sum$**m**(1, 5, 6, 8, 14, 15)

   Attach the duly completed PAL16L8 diagram to your answer book.

   (12 marks)

   (c) Implement the Boolean function, **F4**(w, x, y, z) in part (b) by using a 3-to-8 decoder as given in the Appendix and the minimum number of gates.

   (7 marks)

3. Provide a brief answer for the following questions with justification.

(a) For 2's complement representation of 8-bit size, which of the following values is equal to the decimal value (-49). Justify your answer.

i). $(10110001)_2$ ii). $(11001111)_2$

iii). $(00110001)_2$

(6 marks)

(b) Which of the following binary values is closest to the decimal value $(1.6)_{10}$. Justify your answer.

i). $(1.1)_2$ ii). $(1.011)_2$

iii). $(1.110001)_2$ iv). $(1.101)_2$

(6 marks)

(c) If A = 1, B = 0, and C = 0, then find **X**, where **X** = $\overline{(A \oplus B)} + C$

(3 marks)

(d) Identify the clocked flip-flop described in the following characterization table.

Inputs A	Inputs B	Output Q_{n+1}
0	0	Q_n
1	0	0
0	1	1
1	1	$\overline{Q_n}$

(6 marks)

(e) Considering a 2-Kbyte size memory that facilitates a byte-wide read and write, which of the following information is correct.

i). 2000 address lines and 8 data lines.

ii). 12 address lines and 8 data lines.

iii). 13 address lines and 8 data lines.

iv). 11 address lines and 8 data lines.

Justify your answer

(4 marks)

4. (a) Show how a D-type flip-flop can be constructed by using an SR flip-flop and other logic gates. Draw the complete logic diagram of the circuit.

(6 marks)

(b) Design and implement a 4-bit counter that counts down in sequence (---- 14, 12, 10, 8, 6, 4, 2, 0, 14 -----) by using the minimum number of D-type flip-flops and basic logic gates. Show your complete design with full details including state diagram, state table, simplification of next state equations and a counter with the minimal hardware.

(19 marks)

5. A combinational logic circuit is needed to multiply a 3-bit binary number ($A_2A_1A_0$) by a constant 3_{10}, as shown in Figure Q5.

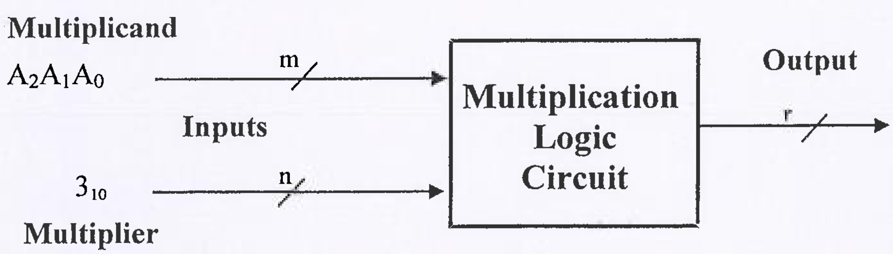


Figure Q5

(a) Determine the number of input and output signals for multiplicand, multiplier and result (m, n and r).

(3 marks)

(b) Construct the truth table of the circuit indicating the input and output variables.

(7 marks)

(c) Simplify the output function using Boolean algebra and write the reduced Boolean functions of the output.

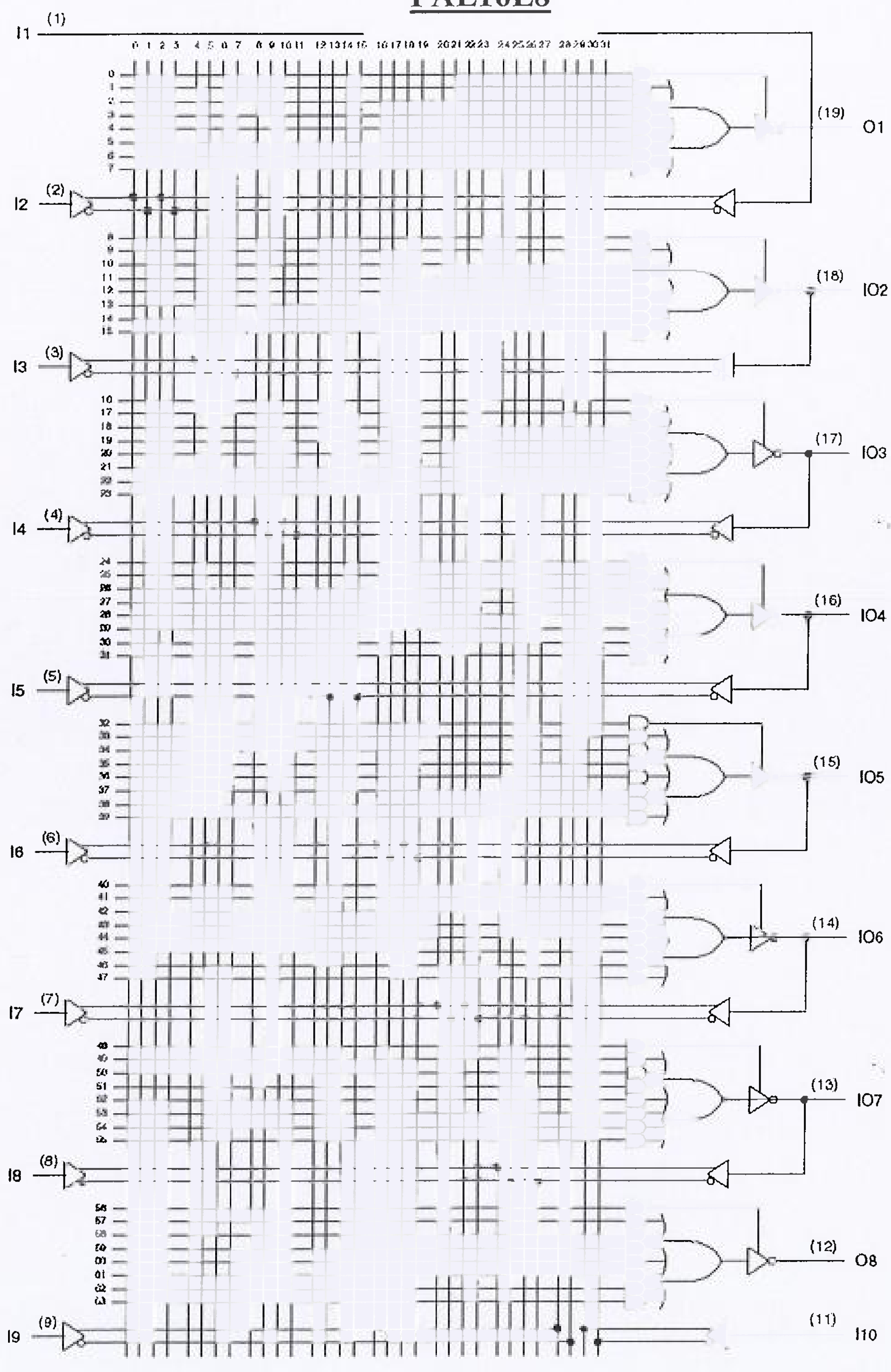
(6 marks)

(d) Simplify the output function using K-map and write the reduced output function. Then implement the Boolean function by using the minimum number of NAND gates.

(9 marks)

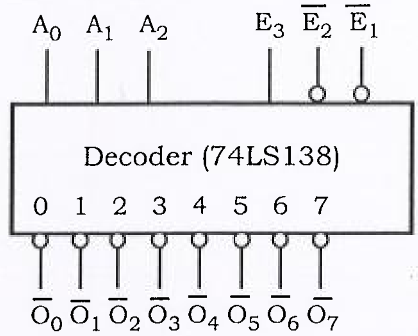
APPENDIX

PAL16L8



Decoder Data Sheet

74LS138: 3-to-8 Decoder



Inputs			
$\overline{E}_1$	$\overline{E}_2$	E_3	
0	0	1	Respond to input code $A_2A_1A_0$
1	x	x	Disabled - all HIGH
x	1	x	Disabled - all HIGH
x	X	0	Disabled - all HIGH