National Exams May 2017

16-Elec-A4, Digital Systems & Computers

3 hours duration

NOTES:

1. If doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumptions made.

2. This is a Closed Book exam.
   Candidates may use one of two calculators, the Casio or Sharp approved models.

3. FIVE (5) questions constitute a complete exam.
   Clearly indicate your choice of any five of the six questions given otherwise the first five answers found will be considered your pick.

4. All questions are worth 12 points.
   See below for a detailed breakdown of the marking.

Marking Scheme

1. (a) 2, (b) 4, (c) 3, (d) 3, total = 12
2. (a) 6, (b) 3, (c) 3, total = 12
3. (a) 8, (b) 4, total = 12
4. (a) 3, (b) 4, (c) 3, (d) 2, total = 12
5. (a) 4, (b) 8, total = 12
6. (a) 3, (b) 3, (c) 3, (d) 3, total = 12

The number beside each part above indicates the points that part is worth

1.- Consider the function

$$f = (A+B)\cdot(B+C)\cdot\left(\overline{A}+\overline{B}+C\right)$$

(a) Synthesize the function f as written above using AND, OR and NOT gates. [2 pts]

(b) Using Boolean algebra put the function into its minimized sum-of-products form and synthesize. [4 pts]

Note: A summary of Boolean algebra identities is provided in a table attached at the end.

(c) Check the results obtained in part (b) by using the K-map method. [3 pts]

(d) Determine if there is a hazard in the minimized function found. Justify your answer. If required modify your minimized function to produce an economic hazard-free implementation. [3 pts]

2.- A 3-bit counter advances through the sequence 000, 001, 011, 100, 110, 111, and repeats.

(a) Using the standard design process, show how to implement this count sequence using D flip-flops. [6 pts]

(b) Sketch the timing diagram for the counter showing its dynamic behavior, include:

- The clock waveform CLK for at least 7 cycles, and
- The output waveforms Q_A, Q_B & Q_C. [3 pts]

(c) Check if the counter is self-starting or if it needs to be initially reset. [3 pts]

Note: Consult the flip-flop excitation table attached at the end as needed.

3.- For the purpose of designing a circuit with inputs X_1, X_0, Y_1 & Y_0, and outputs E & G you are given the following information:

- Output E will be '1' to signal when the sum of binary numbers $X = X_1X_0$ and $Y = Y_1Y_0$ is an even number, otherwise E will be '0'.
- Output G will be '1' to indicate that the sum of 2-bit numbers X & Y is greater than 3, otherwise G will be'0'.

(a) Use K-maps to obtain the minimized sum-of-products expressions for E and G. [8 pts]

(b) Implement the logic circuit using a PAL array. [4 pts]

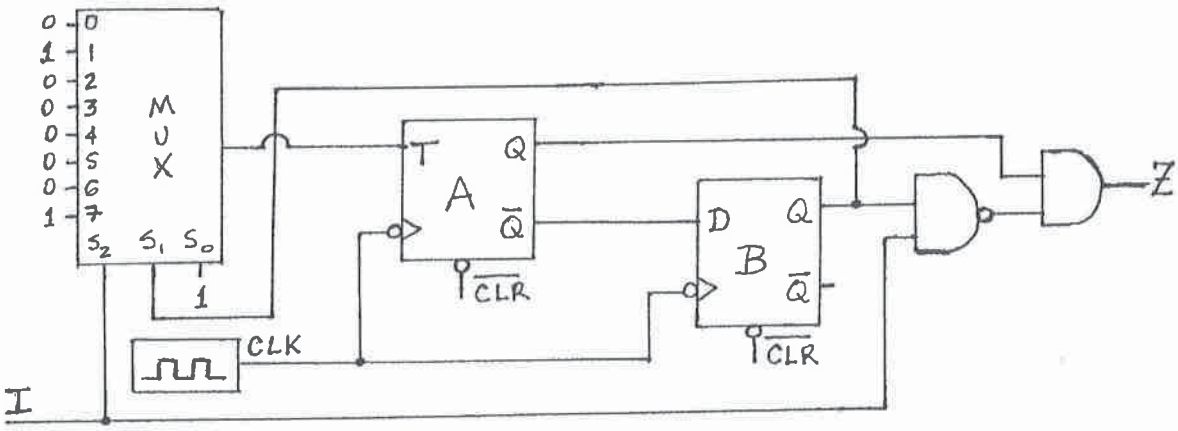
4.- The finite state machine (FSM) shown in the figure below is implemented with one toggle (T) flip-flop and one D flip-flop. It has a single input I and a single output Z. The combinational logic required is implemented by an 8:1 MUX, 1 NAND and 1 AND gates.

(a) Write the logic expressions for T_A, D_B and Z. [3 pts]

(b) Obtain the state transition table including I, Q_A, Q_B, T_A, D_B, Q_A^+, Q_B^+ and Z. [4 pts]

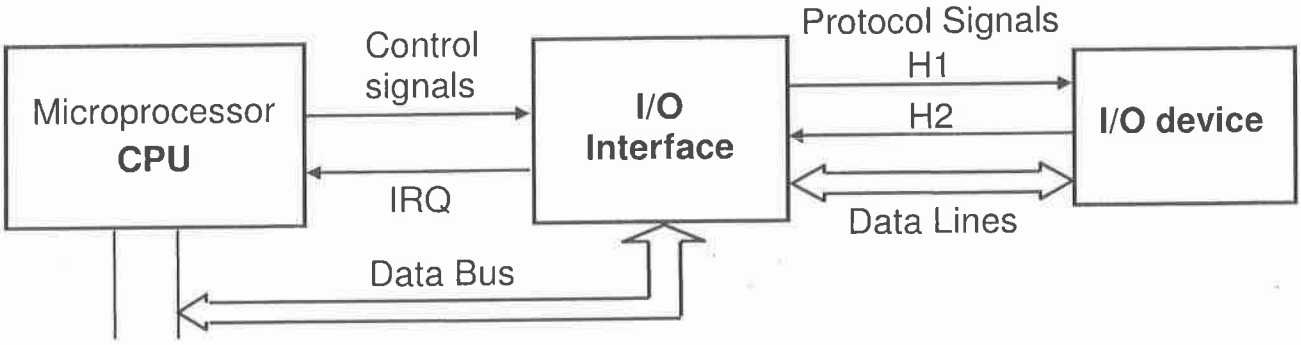
(c) Draw the state transition diagram of the FSM including the I/Z information. [3 pts]

(d) Is this a Moore or a Mealy FSM? Justify. [2 pts]



Note: Consult the flip-flop excitation table attached at the end as needed.

5.- The diagram below shows the main elements participating in the parallel I/O of data.



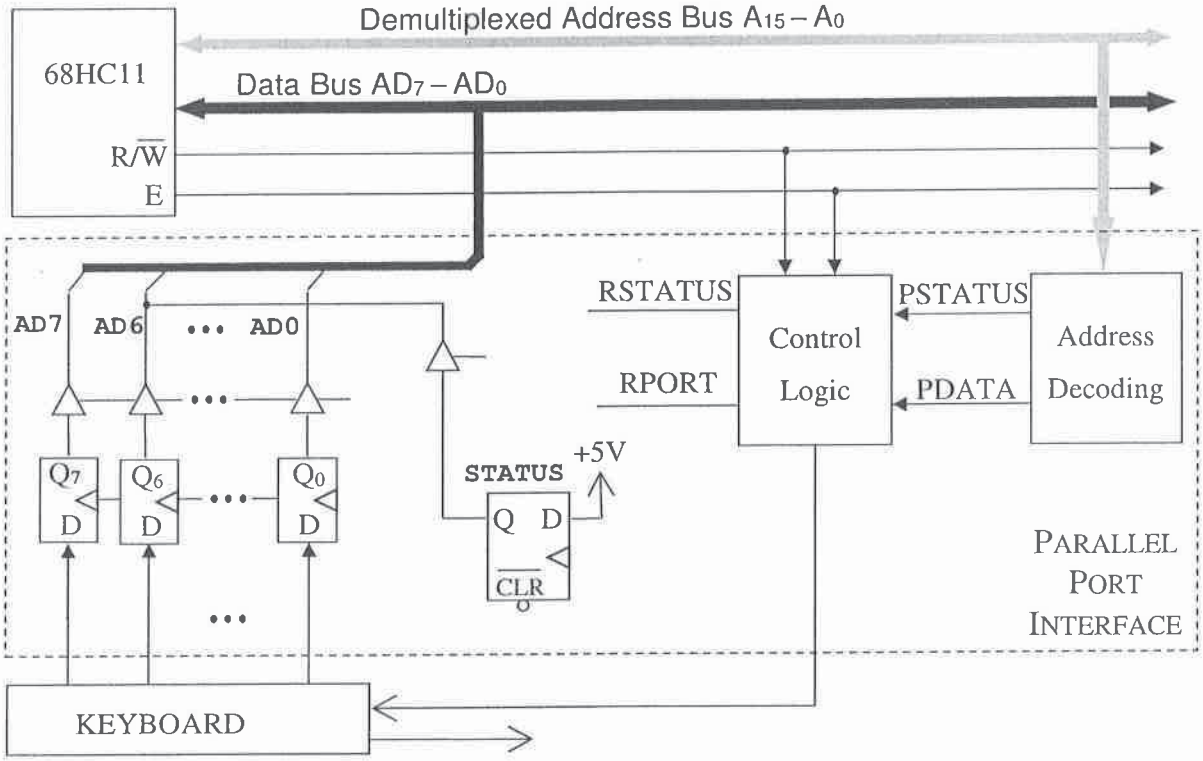
(a) Mention the two methods used in programming the CPU to communicate with the I/O interface in order to become aware of new available data, or interface readiness, and transfer the data between the two in the corresponding direction.

Which of the two methods is more efficient? Explain.

(b) i. Mention two parallel I/O protocols used for implementing the data exchange between the I/O interface and the external I/O device.

ii. Describe the main steps involved in these protocols for the INPUT of data from the I/O device and for the OUTPUT of data to the I/O device, separately.
Mention which protocol signal H1 or H2 work for signaling VALID DATA in data lines or ACKNOWLEDGEMENT of data reception in each case.

6.- Consider the parallel port illustrated in the figure below.



(a) Find Boolean logic expressions to generate the active high signals PSTATUS and PDATA when the address bus contents are $A000 and $A001, respectively.
Use the fewest lines possible. No addresses outside the range $A000-$A7FF should assert PSTATUS or PDATA. [3 pts]

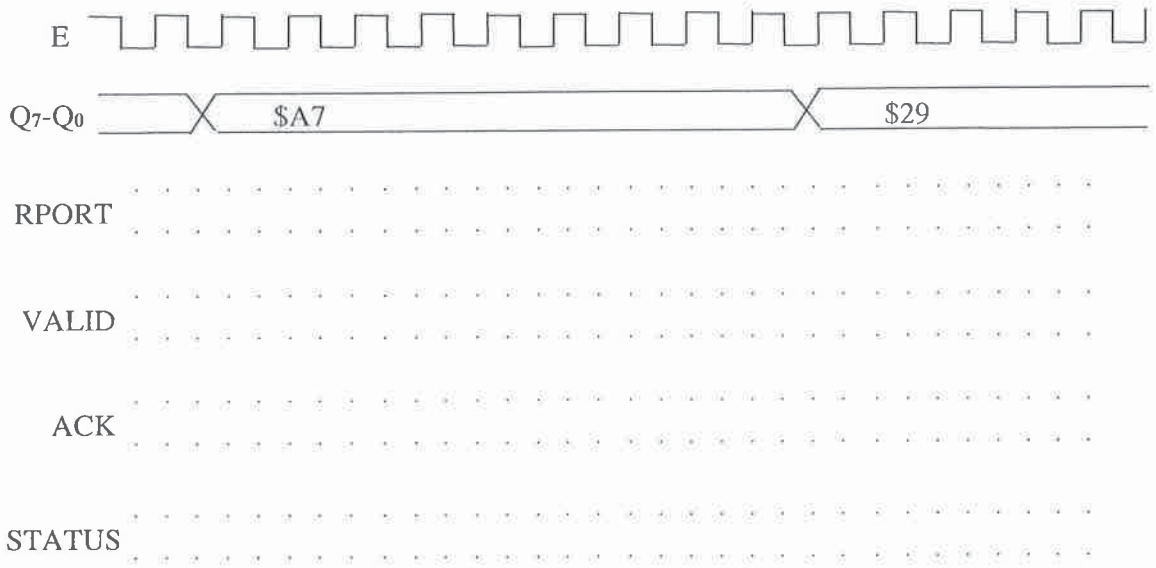
(b) RSTATUS and RPORT are the control signals used by the HC11 to read the status bit and the data register of the parallel port, respectively. Find the Boolean expressions for RSTATUS and RPORT, both to be active high for ½ E clock cycle. [3 pts]

(c) In the diagram above, label the VALID and ACK (acknowledge) lines for the keyboard, connect them to the appropriate places where necessary, and complete all required connections for signals RSTATUS, RPORT and the D flip-flops (the status bit and those in the data register).
Status bit to be set to '1' in order to indicate that new data is available in data register. [3 pts]

(d) In the timing diagram below, sketch waveforms for the signals VALID, ACK, RPORT and the state of the STATUS bit to make them consistent with what is shown on the Q_7-Q_0 data lines of the port interface. Assume interlocked handshake as the control protocol.

Draw arrows indicating which signal:
(1) Causes the change in the data value in Q_7-Q_0, and
(2) Clears the status bit.

All signals are binary (high/low), no need for scale values. [3 pts]



Excitation Table

Q	Q+	R	S	J	K	T	D
0	0	X	0	0	X	0	0
0	1	0	1	1	X	1	1
1	0	1	0	X	1	1	0
1	1	0	X	X	0	0	1

Basic Boolean Identities

	Identity	Comments
1.	$A+0=A$	Operations with 0 and 1
2.	$A+1=1$	Operations with 0 and 1
3.	$A+A=A$	Idompotent
4.	$A+\overline{A}=1$	Complementarity
5.	$A\cdot 0=0$	Operations with 0 and 1
6.	$A\cdot 1=A$	Operations with 0 and 1
7.	$A\cdot A=A$	Idompotent
8.	$A\cdot \overline{A}=0$	Complementarity
9.	$\overline{\overline{A}}=A$	Involution
10.	$A+B=B+A$	Commutative
11.	$A\cdot B=B\cdot A$	Commutative
12.	$A+(B+C)=(A+B)+C=A+B+C$	Associative
13.	$A\cdot(B\cdot C)=(A\cdot B)\cdot C=A\cdot B\cdot C$	Associative
14.	$A\cdot(B+C)=(A\cdot B)+(A\cdot C)$	Distributive
15.	$A+(B\cdot C)=(A+B)\cdot(A+C)$	Distributive
16.	$A+(A\cdot B)=A$	Absorption
17.	$A\cdot(A+B)=A$	Absorption
18.	$(A\cdot B)+(\overline{A}\cdot C)+(B\cdot C)=(A\cdot B)+(\overline{A}\cdot C)$	Consensus
19.	$\overline{A+B+C+\ldots}=\overline{A}\cdot\overline{B}\cdot\overline{C}\cdot\ldots$	De Morgan
20.	$\overline{A\cdot B\cdot C\cdot\ldots}=\overline{A}+\overline{B}+\overline{C}+\ldots$	De Morgan
21.	$(A+\overline{B})\cdot B=A\cdot B$	Simplification
22.	$(A\cdot\overline{B})+B=A+B$	Simplification