National Exams December 2015

98-Comp-A1, Electronics

3 hours duration

NOTES:

1. If doubt exists as to the interpretation of any question, the candidate is urged to indicate, with the answer, a clear statement of any assumptions made.

2. This is a OPEN BOOK exam.
   Any non-communicating calculator is permitted.

3. FIVE (5) questions constitute a complete exam paper.
   The first 5 questions as they appear in the answer book will be marked.

4. Each question is of equal value.

Question 1 (20 marks)

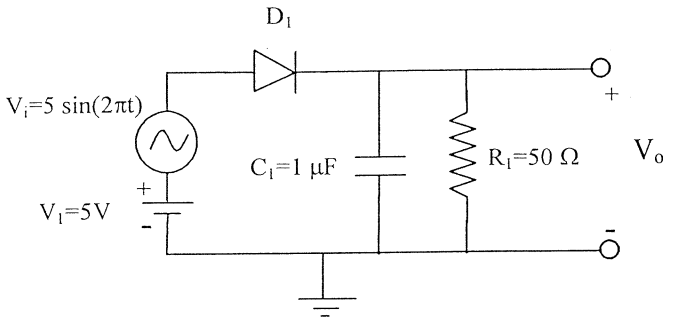

Figure 1. The diode has a voltage drop V_D=0.7V in forward bias.

For the circuit shown in Figure 1:

a) Sketch V_i and V_o as a function of time, indicating peak voltages.

b) Find the maximum and minimum output voltage V_o.

c) What is the peak current through R_1?

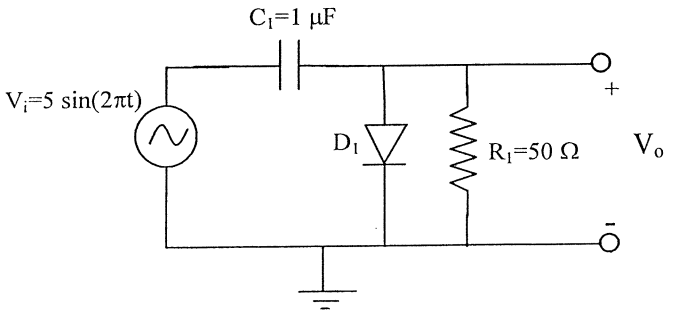

Figure 2. The diode has a voltage drop V_D=0.7V in forward bias.

For the circuit shown in Figure 2:

d)) Sketch the output waveform $V_o(t)$ in steady state. Label peak voltages.

Question 2 (20 marks)

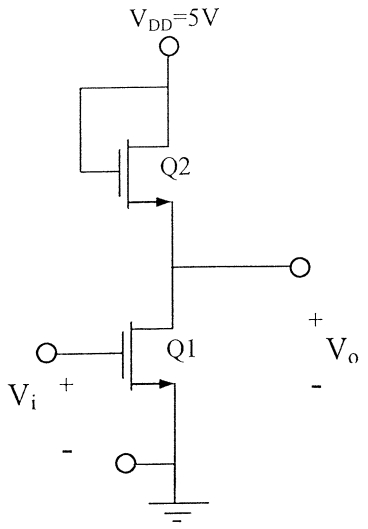

Figure 3. $k_n' = \mu_n C_{ox}$=1 mA/V^2, W/L=10, V_{tn}=1V, $|V_A|$=100V

For the circuit shown in Figure 3:

a) For V_i=2V what is the current through Q1?

b) For V_i=2V, what is V_o?

c) Draw a small signal equivalent model for the circuit.

d) What is the small signal AC gain of the circuit?

Question 3 (20 marks)

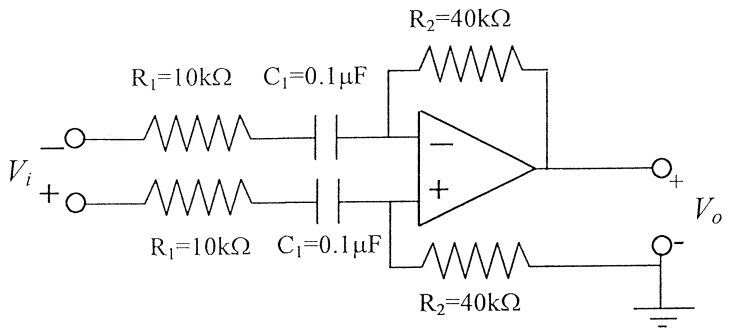

Figure 4.

For the circuit shown in Figure 4:

a) Derive the transfer function $\frac{Vo(j\omega)}{Vi(j\omega)}$ for the circuit shown in Figure 4, assuming the op-amp is ideal.

b) Sketch the frequency response, indicating 3dB frequencies for this circuit.

c) If $V_i(t)$=10sin(120πt) V, find $V_o(j\omega)$.

d) If $V_i(t)$=10sin(120πt) V, find $V_o(t)$.

Question 4(20 marks)

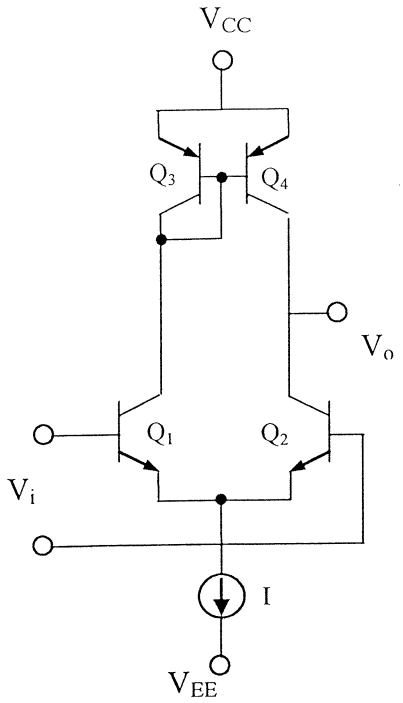

Figure 5. I=0.2mA, β=100, V_A=100V.

For the circuit shown in Figure 5:

a) Find the input resistance Ri.

b) Find the output resistance Ro.

c) Find the amplifier transconductance G_m.

d) Find the open-circuit voltage gain for the amplifier.

Question 5 (20 marks)

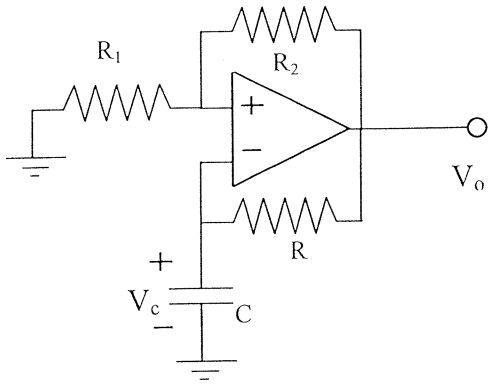

Figure 6. The op-amp saturation voltages are ±12V, R_1=10kΩ, R_2=R=100kΩ, C=0.1μF.

For the circuit shown in Figure 6:

a) Explain the operation of this circuit.

b) Sketch the waveforms $V_c(t)$ and $V_o(t)$.

c) Find an expression for $V_c(t)$.

d) Find the frequency of the output signal V_o.

Question 6 (20 marks)

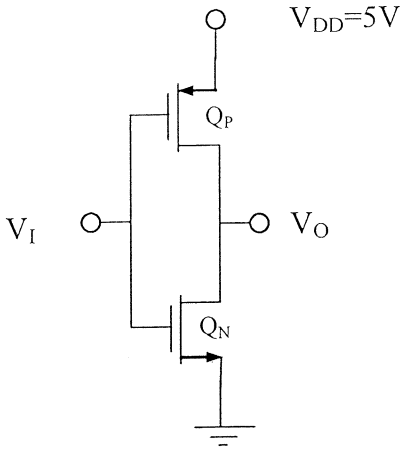

Figure 7. k_n'=50 μA/V^2, k_p'=20 μA/V^2, V_{tn}=-V_{tp}=1V, C_{ox}=1fF/μm^2, V_{DD}=5V
Gate-drain overlap C_{gd}=0.5fF/μm, drain-body C_{db}=10fF, wiring C_{ox}=5fF.

a) If the minimum gate length for this technology is 1 μm, size Q_N and Q_P to obtain a symmetric transfer characteristic.

b) Evaluate the propagation delay for this inverter driving a second identical inverter.

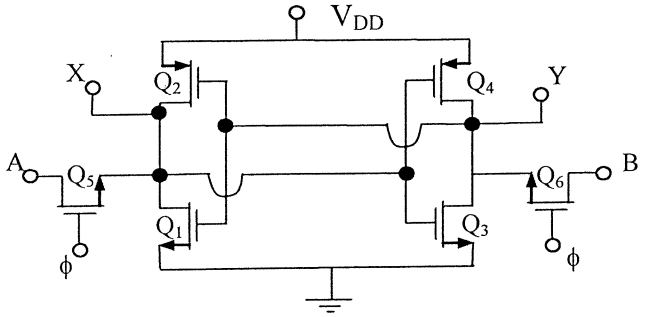

Figure 8.

For the circuit shown in Figure 8:

c) Determine outputs X and Y for all possible inputs A and B. ϕ is a clock signal.

d) If Q_1 and Q_2 are sized as in part a), find a minimum size for Q_5 and Q_6 that will ensure X can be pulled down to V_{DD}/2 or lower.

Question 7 (20 marks)

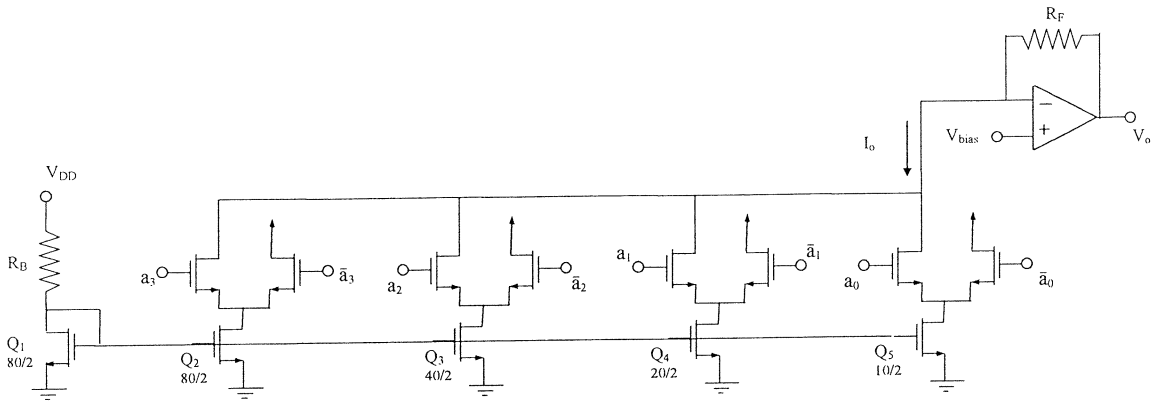

Figure 9. R_B=20kΩ, R_F=5kΩ, V_{DD}=5V, V_{bias}=1V
V_t=0.8V, k'=40 μA/V^2. Transistor dimensions in μm.

a) What is a common name for the circuit shown in Figure 9? Briefly explain how it works.

b) Calculate the drain current for Q_1 (choose a starting value for the gate voltage and iterate to a solution).

c) If a_3-a_0 are connected to V_{DD}, find I_o. For each value of A_{in}=0000 to A_{in}=1111 determine the output V_o.

d) What are the limitations of the application of this circuit?

Marking Scheme

1. 20 marks total (4 parts, 5 marks each)
2. 20 marks total (4 parts, 5 marks each)
3. 20 marks total (4 parts, 5 marks each)
4. 20 marks total (4 parts, 5 marks each)
5. 20 marks total (4 parts, 5 marks each)
6. 20 marks total (4 parts, 5 marks each)
7. 20 marks total (4 parts, 5 marks each)