National Exams May 2019

16-Elec-B5, Advanced Electronics

3 hours duration

Notes:

1. If any doubt exists as to the interpretation of any question, the candidate is urged to submit, within their answer, a clear statement of any assumptions made.

2. This is a **CLOSED BOOK EXAM**. One of two calculators is permitted - any Casio or Sharp approved model.

3. Answer all **FIVE** (5) questions.

4. All questions are worth 20 marks each.

5. Please start each question on a new page and clearly identify the question number and part number, e.g. Q4(a).

6. In schematics, ground and chassis may be assumed to be common, unless specifically stated otherwise.

7. Unless otherwise specified, assume that Op-Amps are ideal and that supply voltages are ±15V.

8. If questions require an answer in essay format, clarity and organization of the answer are important. Provide block diagrams and circuit schematics whenever necessary.

QUESTION (1)

An analog signal in the range 0 to +10 V is to be converted to an 8-bit digital signal.

a) What is the resolution of the conversion in volts? (4 points)

b) What is the digital representation of an input of 6 V? (4 points)

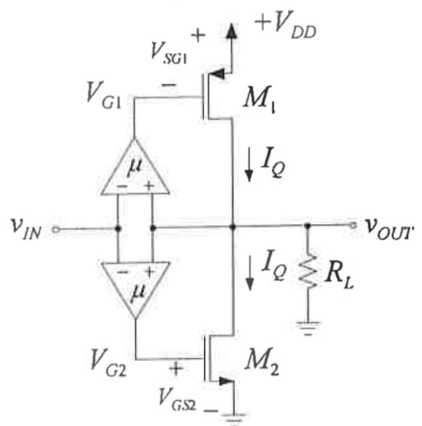
c) What is the representation of an input of 6.2 V? (4 points)

d) What is the error made in the quantization of 6.2 V in absolute terms and in percentage of the input? And as a percent of full scale? (4 points)

e) What is the largest possible quantization error as a percentage of full scale? (4 points)

QUESTION (2)

The following circuit is a class AB power amplifier. The output stage is essentially comprised of two common source amplifiers. The two error amplifiers are used to provide negative feedback to lower the output resistance of this output stage.



Given the followings:

i) Transistors M_1 and M_2 are matched such that $K_n = K_p$, and $V_{Tn} = |V_{Tp}|$

ii) I_Q is the quiescent current for transistors M_1 and M_2 with zero input.

iii) μ is the finite gain of the error amplifiers.

iv) R_L is the load resistance

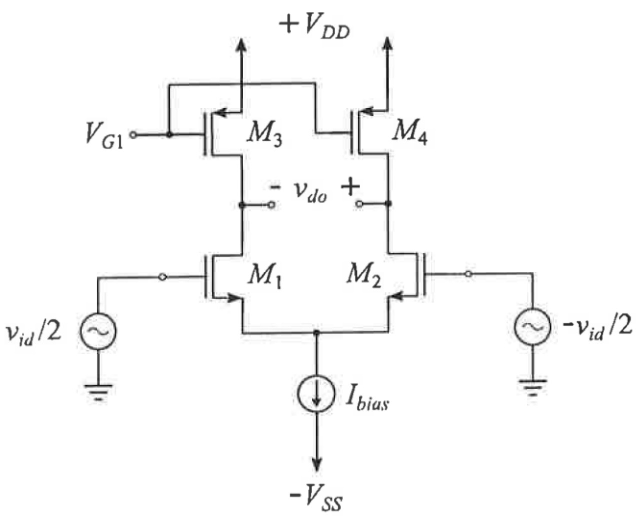
a) Derive an expression for the voltage gain v_{OUT}/v_{IN} of this amplifier? (12 points)

b) What would be the expected gain? (2 points)

c) What would be the gain error? (6 points)

QUESTION (3)

The following single stage differential amplifier circuit is designed for a 0.18 μm CMOS technology.



Given: $V_{DD} = |V_{SS}| = 1.5$ V, $|V_{TH}| = 0.5$ V,
$L = 0.36$ μm (for all transistors),
$\mu_n C_{ox} = 4\mu_p C_{ox} = 400$ μA/V²,
and $\lambda = 0.2$

a) For a bias current of $I_{bias} = 200$ μA and over drive voltage $|V_{ov}| = 0.2$ V for all transistors, determine the W/L ratios for M_1, M_2, M_3, and M_4. (10 points)

b) Determine the small signal differential gain v_{do}/v_{id} for this design. (10 points)

Useful formulae: for n-channel MOSFET

$$i_{DS} = K\left[(v_{GS} - V_{TH})v_{DS} - \frac{1}{2}v_{DS}^2\right] \quad \text{triode region}$$

$$i_{DS} = \frac{1}{2}K(v_{GS} - V_{TH})^2(1 + \lambda v_{DS}) \quad \text{saturation region}$$

$$V_{ov} = V_{GS} - V_{TH} \quad \text{overdrive voltage}$$

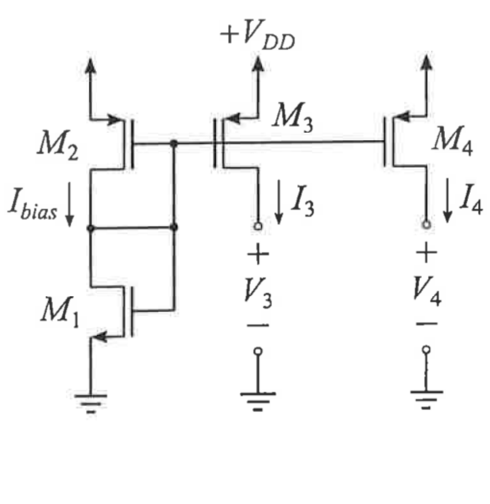
where

$$K = K'\left(\frac{W}{L}\right) = \mu C_{ox}\left(\frac{W}{L}\right)$$

$$V_A = \frac{1}{\lambda}, \text{ and } V_A = V_A' L, \; r_o = \frac{1}{\lambda I_D}$$

QUESTION (4)

This following current mirror circuit is used to provide bias currents I_3 and I_4 to other circuit blocks.



Given: $V_{DD} = 3.0$ V, $|V_{TH}| = 0.5$ V,
$L = 0.36$ μm (for the p-channel transistors),
$\mu_n C_{ox} = 4\mu_p C_{ox} = 400$ μA/V²,
and $\lambda = 0.2$

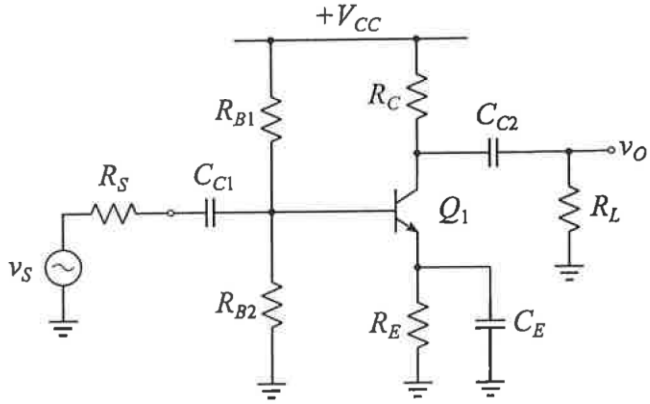
a) For a bias current of $I_{bias} = 200$ μA and over drive voltage $|V_{ov}| = 0.3$ V for all the p-channel transistors, determine the W/L ratios for M_1, and M_2. Note that the channel length for transistor M1 can be 0.36 μm or longer. (8 points)

b) Determine the W/L ratios for M_3, and M_4 for $I_3 = 4 \times I_4 = 8 \times I_{bias}$. (2 points)

c) Determine the variation in I_3 if the voltage V_3 swings from 0 to 1.5 V. (10 points)

QUESTION (5)

The following common emitter amplifier is already biased properly. Determine the appropriate values for C_{C1}, C_{C2}, C_E to provide a lower cutoff frequency of f_L = 100 Hz. Which capacitor dominates this corner frequency? (20 points)



Given: R_{B1} = 180 kΩ,
R_{B2} = 270 kΩ,
R_S = 5 kΩ,
R_C = 8 kΩ,
R_E = 2 kΩ,
R_L = 5 kΩ,
β = 100,
g_m = 40 mA/V, and
r_π = 2.5 5 kΩ.