National Exams May 2016

07-Elec-A4, Digital Systems & Computers

3 hours duration

NOTES:

1. If doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumptions made.

2. This is a Closed Book exam.
   Candidates may use one of two calculators, the Casio or Sharp approved models.

3. FIVE (5) questions constitute a complete exam.
   Clearly indicate your choice of any five of the six questions given otherwise the first five answers found will be considered your pick.

4. All questions are worth 12 points.
   See below for a detailed breakdown of the marking.

Marking Scheme

1. (a) 2, (b) 5, (c) 2, (d) 3, total = 12
2. (a) 3, (b) 6, (c) 3, total = 12
3. (a) 2, (b) 4, (c) 2, (d) 4, total = 12
4. (a) 4, (b) 5, (c) 3, total = 12
5. (a) 4, (b) 4, (c) 4, total = 12
6. (a) 4, (b) 8, total = 12

The number beside each part above indicates the points that part is worth

1.- Given the following function in sums-of-product (SoP) form:

$$f(A, B, C, D) = \sum m_i (0,1,2,4,5,6,7,8,10)$$

where m_i represent the minterms involved in the SoP canonical form of f.

(a) Prepare its truth table.

(b) Map the function f in a K-map and identify:

   i. One implicant that is not a prime implicant,

   ii. One prime implicant that is not essential, and

   iii. All essential prime implicants.

   In identifying each implicant above list all the minterms in each of them.

(c) Write the minimized SoP form for f.

(d) Is the minimized SoP expression found hazard-free?
   Explain and if it is not provide the hazard-free SoP form for f.

2.- The following circuit contains two JK flip-flops.

(a) Write the logic expressions for J_A, K_A, J_B and K_B.   [3 pts]

(b) Obtain the state transition table for the circuit.   [6 pts]

(c) Sketch the state transition diagram for the circuit.   [3 pts]
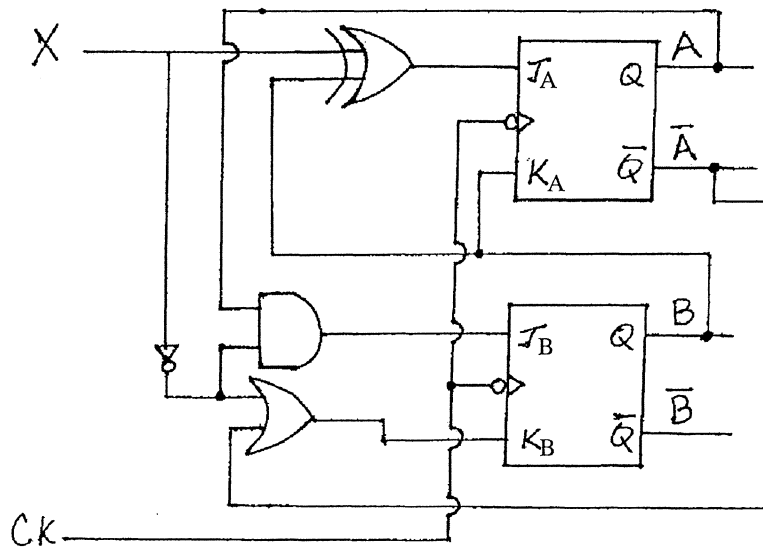
Note: Consult the flip-flop excitation table attached at the end as needed.

3.- (a) Provide the state transition table for an asynchronous binary up-counter that will go through the sequence 0000, 0001, 0010, ..., 1111, 0000, ...

(b) Build the asynchronous binary up-counter in (a) using T flip-flops.

(c) Provide the state transition table for a decade counter.

(d) Build an asynchronous decade binary up-counter using T flip-flops.

Hint: Try modifying the counter in (b) such that it turns into a decade counter.

4.- The figure below shows a memory cell A built using two cascaded inverters. Data input D contains the value to be written to the memory cell. Control input $\overline{W}$ (write) determines when the value of the memory cell is to be updated with the value in D. Two tri-state gates (buffers) are used for this purpose.
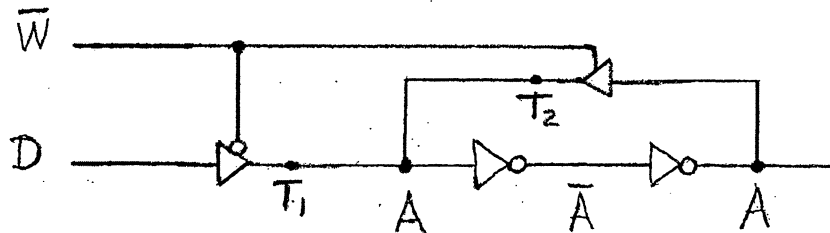
(a) Is the control input $\overline{W}$ (write) active-low or active-high?
Explain by describing how the value of the cell is (i) held and (ii) updated.

(b) Provide a truth table having A, D and $\overline{W}$ as inputs, and showing the values of the 2 tri-state gate outputs T_1 and T_2 for each input combination.

(c) How long does $\overline{W}$ have to be active for the memory update to be successful? Explain.

5.- (a) Identify by marking with a X which of the following are the 4 essential components of a computer system.

    __ Mouse   __ Busses (address, data, control)

    __ Processor (CPU)   __ Keyboard

    __ Printer   __ Display monitor

    __ Hard drive   __ I/O ports

    __ Memory

(b) Identify the main differences between a general purpose microprocessor and a microcontroller.

(c) Identify which CPU register(s) is(are) typically associated with each of the following

    - the address of the next instruction to be executed : _____

    - the next available location at the top of the stack : _____

    - pointing to an array or list of data values in memory : _____

    - containing the information an assembly program uses at decision making points (conditional branch statements): _____

6.- Figure 6.1 below shows a circuit used to display six BCD digits in six common-cathode seven-segment displays. The LED arrangement for each seven-segment display is shown in parts 6.2 and 6.3 of the figure. A buffer chip is used to provide the current required to light up the LEDs as determined by Port B pin values, *i.e.* it provides all six displays with a logic '0' or a logic '1' as dictated by PB_7-PB_0, while adding the required driving capacity.

(a) Using a CPU accumulator register A with 'ldaa' (load accumulator A) and 'staa' (store accumulator A) instructions available, write a sequence of assembly instructions to display the number '6' on the seven-segment display #0.

Port B and Port D are memory mapped with addresses $1004 and $1008, respectively.

(b) Describe a way through which we can observe not just one digit lit as in part (a) above but all digits simultaneously showing '09.05.16' on the display arrangement shown in Figure 6.1. Include the sequence of steps to accomplish this as well as the bit patterns needed for Port B.

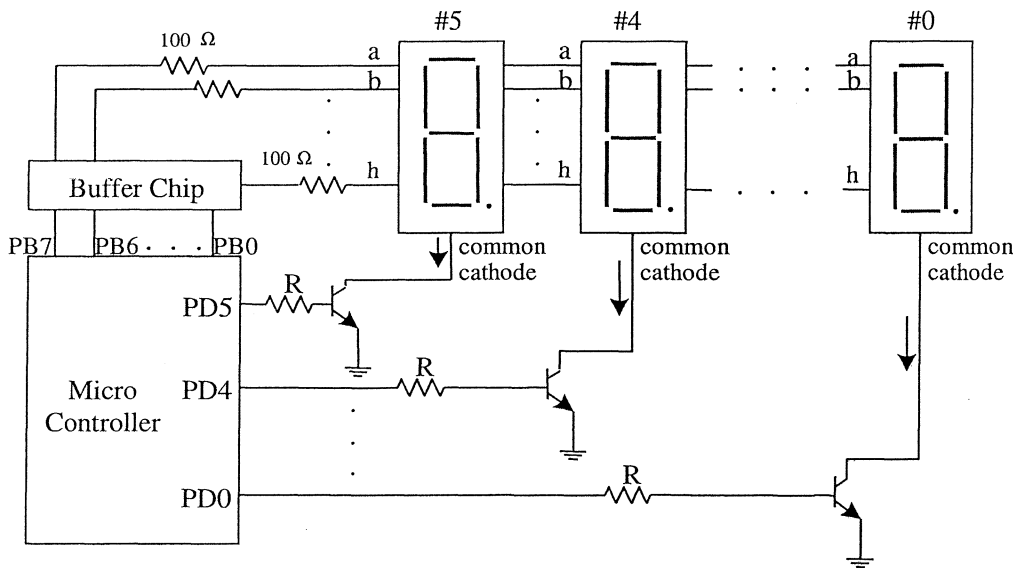*No need to include assembly instructions in part (b) just the algorithmic sequence.*

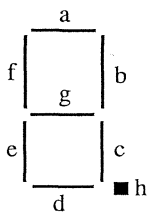Fig 6.1. Port B and Port D together drive six seven-segment displays
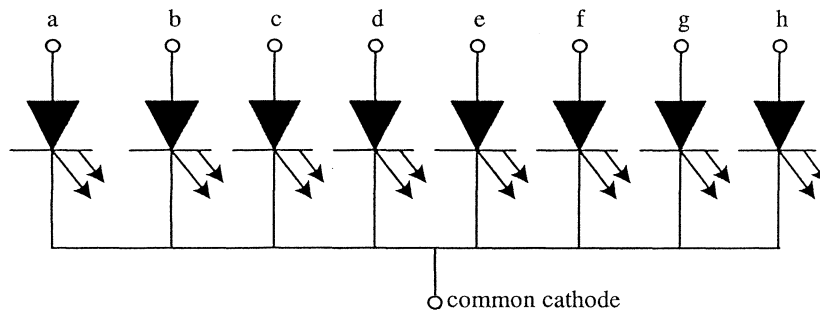

Fig 6.2. Seven-segment display

Fig 6.3. Common-cathode seven-segment display

Excitation Table

Q	Q+	R	S	J	K	T	D
0	0	X	0	0	X	0	0
0	1	0	1	1	X	1	1
1	0	1	0	X	1	1	0
1	1	0	X	X	0	0	1

Basic Boolean Identities

	Identity	Comments
1.	$A + 0 = A$	Operations with 0 and 1
2.	$A + 1 = 1$	Operations with 0 and 1
3.	$A + A = A$	Idompotent
4.	$A + \overline{A} = 1$	Complementarity
5.	$A \cdot 0 = 0$	Operations with 0 and 1
6.	$A \cdot 1 = A$	Operations with 0 and 1
7.	$A \cdot A = A$	Idompotent
8.	$A \cdot \overline{A} = 0$	Complementarity
9.	$\overline{\overline{A}} = A$	Involution
10.	$A + B = B + A$	Commutative
11.	$A \cdot B = B \cdot A$	Commutative
12.	$A + (B + C) = (A + B) + C = A + B + C$	Associative
13.	$A \cdot (B \cdot C) = (A \cdot B) \cdot C = A \cdot B \cdot C$	Associative
14.	$A \cdot (B + C) = (A \cdot B) + (A \cdot C)$	Distributive
15.	$A + (B \cdot C) = (A + B) \cdot (A + C)$	Distributive
16.	$A + (A \cdot B) = A$	Absorption
17.	$A \cdot (A + B) = A$	Absorption
18.	$(A \cdot B) + (\overline{A} \cdot C) + (B \cdot C) = (A \cdot B) + (\overline{A} \cdot C)$	Consensus
19.	$\overline{A + B + C + ...} = \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot ...$	De Morgan
20.	$\overline{A \cdot B \cdot C \cdot ...} = \overline{A} + \overline{B} + \overline{C} + ...$	De Morgan
21.	$(A + \overline{B}) \cdot B = A \cdot B$	Simplification
22.	$(A \cdot \overline{B}) + B = A + B$	Simplification