National Exams May 2019

04-BS-8, Digital Logic Circuits

3 hours duration

NOTES:

1. If a doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumption made with the answer of the question.

2. Candidates may use one of the two calculators, the Casio or Sharp approved models. This is a closed book examination. However, candidates can bring one hand-written information sheet (8.5" X 11" size double sided) of self-prepared notes.

3. This paper contains **FIVE (5)** questions and comprises **five (5)** pages.

4. Any **FOUR (4)** questions constitute a complete paper. Only the first four questions as they appear in your answer book will be marked.

5. All questions are of equal marks. Total marks = 100.

6. Each question carries 25 marks and the marks for each part of the questions are indicated in brackets.

7. A PAL16R4 Data sheet is provided in the Appendix. It can be used to provide the solution of Question 1, part (c) and should be attached to your answer sheet.

1. A combination lock employs a clocked synchronous sequential circuit. Design the sequential circuit that has a serial input, **Y** and one output, $\overline{LOCK}$ as shown in Figure Q1. The output $\overline{LOCK}$ should be 0 if and only if, **Y** is 0 and the sequence of inputs received at **Y** for the preceding four clock ticks were 1011.

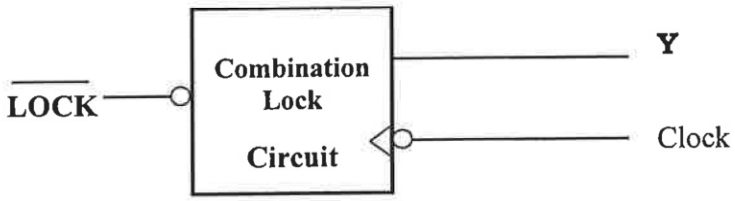


Figure Q1

(a) Draw the state diagram of the sequential machine used in the combination lock.

(5 marks)

(b) Design the sequential circuit by employing D-type flip-flops.

(12 marks)

(c) Implement the Lock circuit design of part (b) by using a PAL16R4 device whose data sheet is given in the Appendix. Show the intact PAL fuses by crossing them in the diagram.

(8 marks)

2. A traffic light controller is required to simulate a traffic light system. The controller has three active-low outputs that drive green, yellow and red LEDs respectively to emulate the following traffic light sequence repeatedly:

- Green LED on for 14 seconds.
- Both Yellow and Green LEDs on for 4 seconds.
- Red LED on for 12 seconds.

Design the controller by using a suitable size counter and some other logic such as decoders, etc. Assume that a clock signal of 1 Hz is available. Assume that suitable binary counters, decoders as well as logic gates and flip-flops are available.

(25 marks)

3. Design a synchronous counter that has the following odd number sequence (1, 3, 5, 7, 9, 11, 13, 15 & repeat). Use negative edge triggered flip-flops of your choice and logic gates to implement the counter.

(a) Your counter design process may start with a state table.

(5 marks)

(b) Determine the next state equations and simplify them if required. Show your complete work.

(12 marks)

(c) Implement and draw the synchronous counter circuit.

(8 marks)

4. (a) Determine the Boolean expression for output **X** of the circuit given in Figure Q4. Simplify the expression using Boolean algebra.

(6 marks)

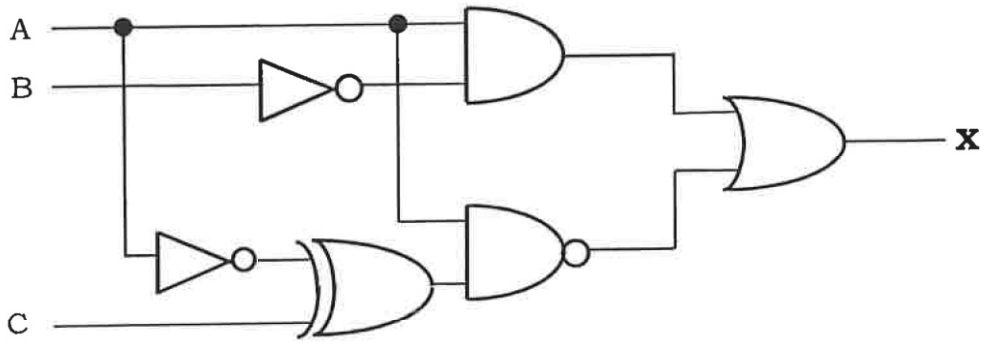


Figure Q4

(b) Simplify the switching function, **Y** by using K-map method.
Y(A, B, C, D) = Π**M** (1, 2, 4, 5, 6, 7, 10, 11, 15)

(i) Draw the K-map for the function, **Y**.
(ii) Simplify the switching function, **Y** and write its simplified Boolean expression in product of sum (POS) form.
(iii) Implement the minimized expression of **Y**(A, B, C, D) by using only NOR gates.

(4+8+7 marks)

5. (a) Synthesize the JK flip-flop circuit of Figure Q5 given below.

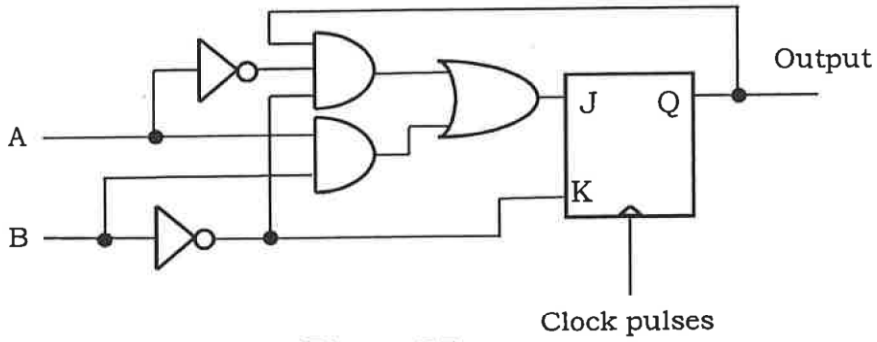


Figure Q5

Determine the output, Q at positive clock transitions for all the combinations of inputs, A and B.

(10 marks)

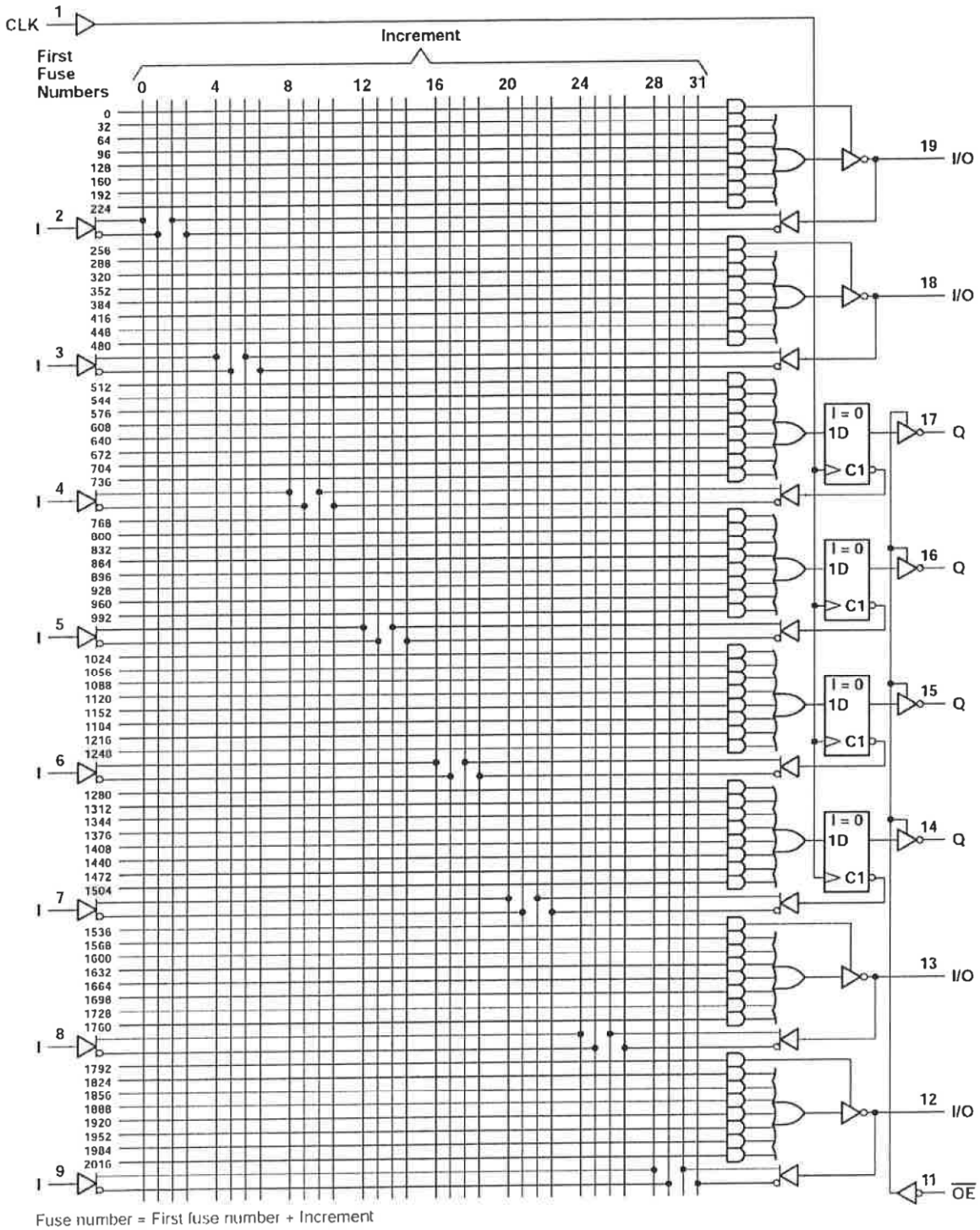
(b) Design a combinational logic circuit to convert 4-bit negative binary numbers into their 2's complement representation. You can use any type and number of combinational logic gates.

(15 marks)

End of Questions

APPENDIX

PAL16R4



End of Paper