National Exams December 2016

07-Elec-A4, Digital Systems & Computers

3 hours duration

NOTES:

1. If doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumptions made.

2. This is a Closed Book exam.
   Candidates may use one of two calculators, the Casio or Sharp approved models.

3. FIVE (5) questions constitute a complete exam.
   Clearly indicate your choice of any five of the six questions given otherwise the first five answers found will be considered your pick.

4. All questions are worth 12 points.
   See below for a detailed breakdown of the marking.

Marking Scheme

1. (a) 3, (b) 3, (c) 3, (d) 3, total = 12
2. (a) 3, (b) 6, (c) 3, total = 12
3. (a) 6, (b) 6, total = 12
4. (a) 4, (b) 3, (c) 5, total = 12
5. (a) 5, (b) 7, total = 12
6. (a) 4, (b) 4, (c) 4, total = 12

The number beside each part above indicates the points that part is worth

1.- Given the following function in product-of-sums (PoS) form:

$$f(A,B,C,D) = (B+\overline{C})\cdot(\overline{A}+\overline{B}+C)\cdot(B+C+D)$$

(a) Prepare its truth table. [3 pts]

(b) Express f in canonical sum of products (SoP) form using the abbreviated notation involving minterms, *i.e.*, $f(A,B,C,D) = \sum m_i\,(\ldots)$ [3 pts]

(c) Map the function f in a Karnaugh map (K-map) and find the minimized SoP form. [3 pts]

Note: Alternatively you can verify this result using Boolean algebra, a summary of identities is provided in a table attached at the end.

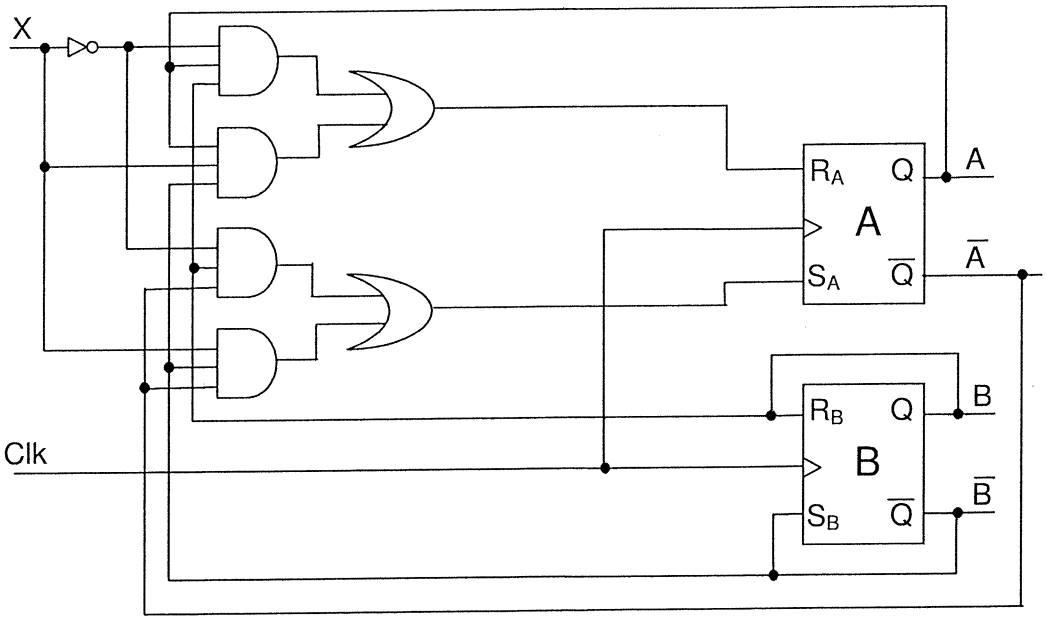
(d) Is the expression found in part (c) hazard-free? If not, give the hazard-free SoP form. [3 pts]

2.- The following circuit contains two RS flip-flops.

(a) Write the logic expressions for R_A, S_A, R_B and S_B. [3 pts]

(b) Obtain the state transition table for the circuit. [6 pts]

(c) Sketch the state transition diagram for the circuit. [3 pts]



Note: Consult the flip-flop excitation table attached at the end as needed.

3.- The following is a truth table of a 3-input, 4-output combinational circuit.

(a) Using K-maps obtain the simplified expressions for A, B, C and D. [6 pts]

(b) Implement using a PAL or PLA architecture. Justify your choice. [6 pts]

Inputs			Outputs			
X	Y	Z	A	B	C	D
0	0	0	0	1	1	0
0	0	1	1	0	0	0
0	1	0	0	0	1	1
0	1	1	1	1	1	1
1	0	0	1	0	1	1
1	0	1	0	1	0	1
1	1	0	0	1	1	0
1	1	1	1	1	0	1

4.- (a) A NOR gate can be used single-handedly to implement any of the three basic logic gates. Show this by drawing the circuits for the AND, OR & NOT gates. [4 pts]

(b) A combinational circuit is formed by a combination of logic gates that produce an immediate change in the output when inputs change. How is this different in the case of sequential circuits? Explain. [3 pts]

(c) i. Draw the circuit of a synchronous counter.

ii. Draw the circuit of an asynchronous counter.

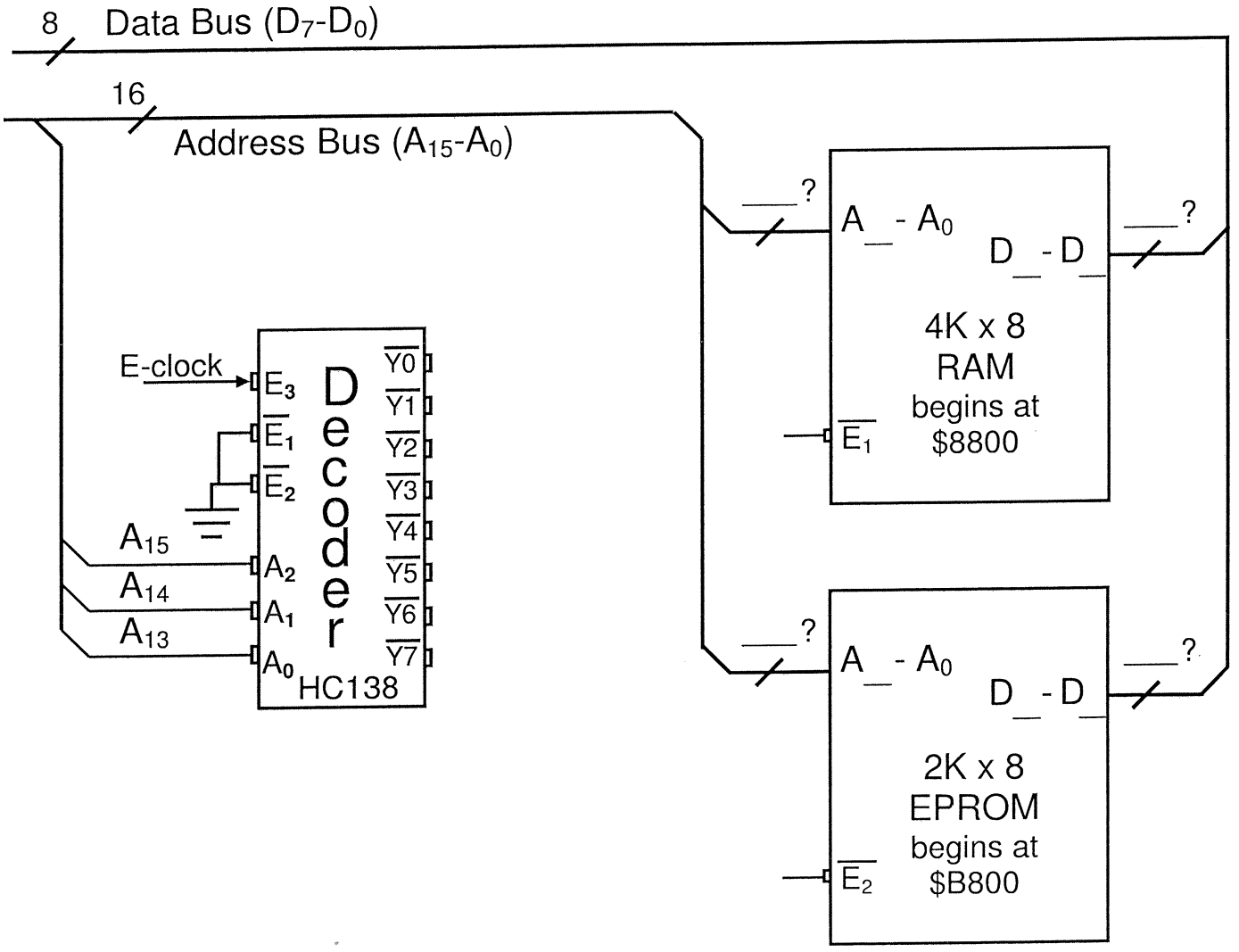
Clearly identify each of them and justify why one is synchronous and not the other. [5 pts]

5.- Two new external memory chips need to be added to a microprocessor system – a 4Kbyte RAM that should begin at $8800, and a 2Kbyte EPROM that should begin at $B800. Regions $9800-$9FFF, $B600-$B7FF & $C000-$FFFF of the memory map are in use already and conflict should be avoided.

(a) Fill in the blanks *beside* and *inside* the memory chips with the appropriate numbers. The number on top of this symbol —/— represents the number of lines on that bus. [5 pts]

(b) $\overline{E_1}$ & $\overline{E_2}$ are the active-low chip select pins for the RAM & EPROM chips, respectively. Find their Boolean expressions. Use the minimum number of lines and gates possible. Use decoder outputs to minimize decoding logic. Complete the connections in the figure below (adding logic gates where needed) to create the address decoding specified. [7 pts]

Note: The '$' sign indicates the number following it is a hexadecimal number.

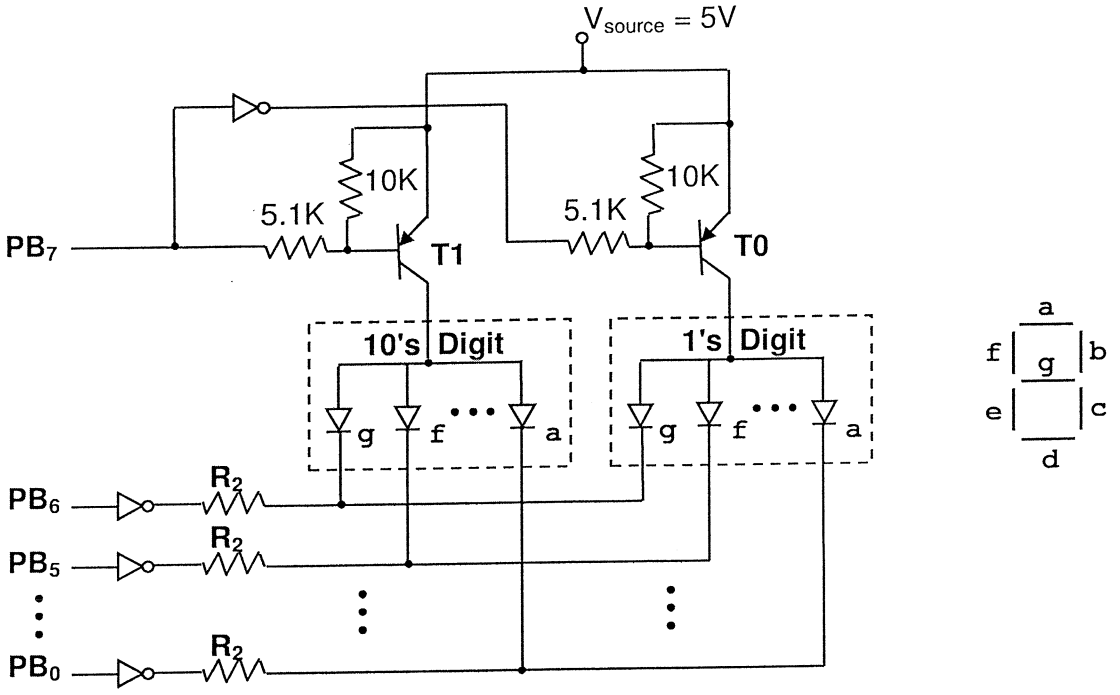


6.- The figure below shows a circuit used to display two digits in two common-anode seven-segment LED displays. The LED arrangement for each seven-segment display is shown on the right side. Parallel Port B lines PB_7-PB_0 of a microcontroller are used to control the two-digit display. PB_7 is used for digit selection, while PB_6-PB_0 are used to determine which segments are lit. Consider that inverters are open-collector TTL inverters and transistor saturation V_{CE} value is approximately 0.3V.

i. Provide the binary values needed in Port B lines to display: [4 pts]
(i) the number '3' in the 10's digit, and
(ii) the number '6' in the 1's digit.

ii. From the programming point-of-view suggest the sequence of steps that will allow observing the number '36' lit on the 2-digit display. Explain. [4 pts]

iii. Find the value for the resistors R_2 that will allow limiting the current through each LED to 10mA. When turned on, consider the nominal voltage across a LED is 2V. [4 pts]



Excitation Table

Q	Q+	R	S	J	K	T	D
0	0	X	0	0	X	0	0
0	1	0	1	1	X	1	1
1	0	1	0	X	1	1	0
1	1	0	X	X	0	0	1

Basic Boolean Identities

	Identity	Comments
1.	$A+0=A$	Operations with 0 and 1
2.	$A+1=1$	Operations with 0 and 1
3.	$A+A=A$	Idompotent
4.	$A+\overline{A}=1$	Complementarity
5.	$A\cdot 0=0$	Operations with 0 and 1
6.	$A\cdot 1=A$	Operations with 0 and 1
7.	$A\cdot A=A$	Idompotent
8.	$A\cdot \overline{A}=0$	Complementarity
9.	$\overline{\overline{A}}=A$	Involution
10.	$A+B=B+A$	Commutative
11.	$A\cdot B=B\cdot A$	Commutative
12.	$A+(B+C)=(A+B)+C=A+B+C$	Associative
13.	$A\cdot(B\cdot C)=(A\cdot B)\cdot C=A\cdot B\cdot C$	Associative
14.	$A\cdot(B+C)=(A\cdot B)+(A\cdot C)$	Distributive
15.	$A+(B\cdot C)=(A+B)\cdot(A+C)$	Distributive
16.	$A+(A\cdot B)=A$	Absorption
17.	$A\cdot(A+B)=A$	Absorption
18.	$(A\cdot B)+(\overline{A}\cdot C)+(B\cdot C)=(A\cdot B)+(\overline{A}\cdot C)$	Consensus
19.	$\overline{A+B+C+\ldots}=\overline{A}\cdot\overline{B}\cdot\overline{C}\cdot\ldots$	De Morgan
20.	$\overline{A\cdot B\cdot C\cdot\ldots}=\overline{A}+\overline{B}+\overline{C}+\ldots$	De Morgan
21.	$(A+\overline{B})\cdot B=A\cdot B$	Simplification
22.	$(A\cdot\overline{B})+B=A+B$	Simplification