National Exams May 2018

16-Elec-A4, Digital Systems & Computers

3 hours duration

NOTES:

1. If doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumptions made.

2. This is a Closed Book exam.
   Candidates may use one of two calculators, the Casio or Sharp approved models.

3. FIVE (5) questions constitute a complete exam.
   Clearly indicate your choice of any five of the six questions given otherwise the first five answers found will be considered your pick.

4. All questions are worth 12 points.
   See below for a detailed breakdown of the marking.

Marking Scheme

1. (a) 2, (b) 2, (c) 2, (d) 3, (e) 3, total = 12
2. (a) 9, (b) 3, total = 12
3. (a) 2.5, (b) 4.5, (c) 3, (d) 2, total = 12
4. (a) 3, (b) 3, (c) 6, total = 12
5. (a) 4, (b) 8, total = 12
6. (a) 4, (b) 8, total = 12

The number beside each part above indicates the points that part is worth

1.- A combinational circuit taking a nonnegative three digit binary number ABC as input decides whether it is an even number or the two most significant digits A & B are equal (indicating it with output E = 1) and whether the sum of its two least significant digits B & C is odd (indicating it with output O = 1).

(a) Provide the truth table for the circuit.

(b) Write output E in canonical sum-of-products (SoP) form.

(c) Write output O in canonical product-of-sums (PoS) form.

(d) Use Boolean identities to find the minimized SoP form for output E.

(e) Use Boolean identities to find the minimized PoS form for output O.

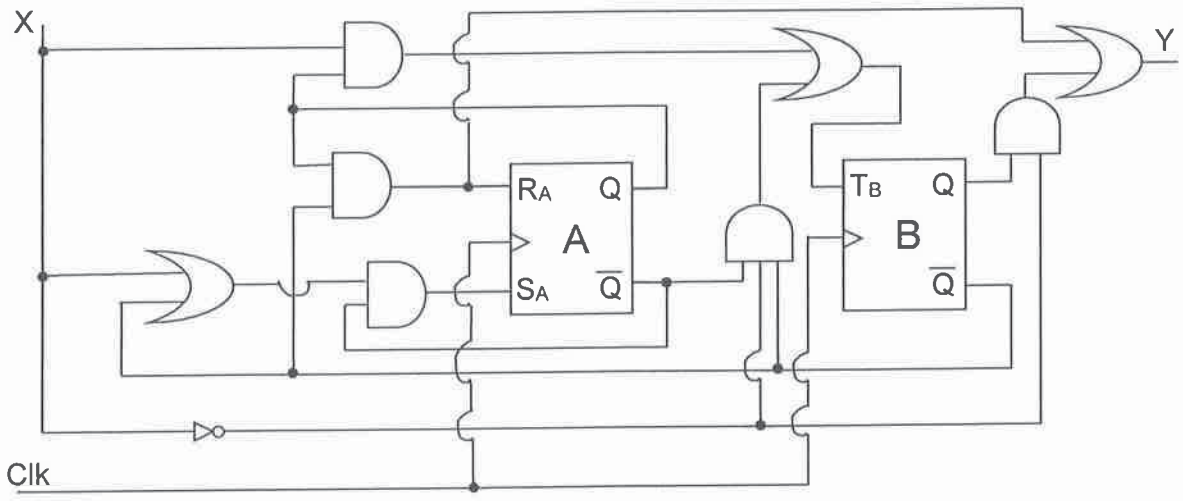
Note: Please find a table with Boolean identities attached in the last page

2.- A circuit is needed to start and stop counting clock pulses on command.

(a) Design a 3-bit synchronous counter that goes through the sequence 000, 001, 010, 011, 100, 101, 110, 111 and then repeats. Use positive-edge-triggered JK flip-flops. Label the bits Q_C, Q_B & Q_A where Q_C is the most significant bit.
Draw the circuit implementing the counter.

(b) Modify the circuit so that it counts whenever an additional COUNT ENABLE (CTE) input is HIGH, stops counting when CTE goes LOW and resumes counting from where it stopped when CTE goes HIGH again.

3.- The following circuit with input X and output Y uses one RS flip-flop and a T flip-flop.



(a) Write the logic expressions for R_A, S_A, T_B and Y.

(b) Obtain the state transition table for the circuit.

(c) Sketch the state transition diagram for the circuit.

(d) Is this a Moore or a Mealy machine? Explain.

Note: Consult flip-flop excitation tables attached at the end as needed.

4.- (a) Where is the use of a parallel-to-serial shift register needed, in the receiving unit of a serial communication port or in its transmitting unit? Explain.

(b) Where is the use of a serial-to-parallel shift register needed, in the receiving unit of a serial communication port or in its transmitting unit? Explain.

(c) Draw the circuit for a 4-bit shift register using D flip-flops that can perform parallel-to-serial conversion as well as serial-to-parallel conversion.

In your diagram, identify:

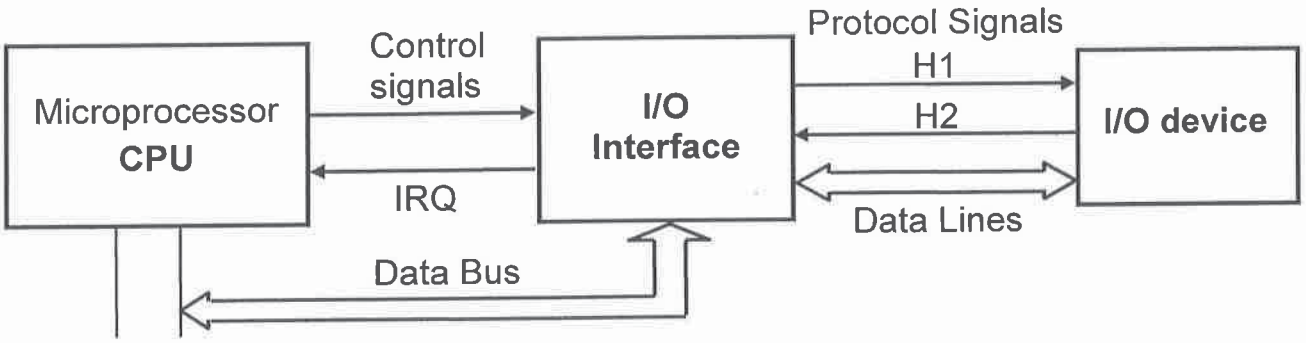
i) The serial input terminal,

ii) The serial output terminal,

iii) The parallel input terminals, and

iv) The parallel output terminals.

5.- The diagram below shows the main elements participating in the parallel I/O of data.



(a) Mention the names of two commonly used methods for the CPU to communicate with the I/O interface.

(b) i. Mention three different parallel protocols used for implementing the data exchange between the I/O interface and the external I/O device.

ii. Mention the common names for protocol signals H1 and H2 associated with each protocol and describe how they are used in the input protocols and in the output protocols separately.

6.- Figure 6.1 below shows a circuit used to display six BCD digits in six common-cathode seven-segment displays. The LED arrangement for each seven-segment display is shown in parts 6.2 and 6.3 of the figure. A buffer chip is used to provide the current required to light up the LEDs as determined by Port B pin values, *i.e.* it provides all six displays with a logic '0' or a logic '1' as dictated by PB_7-PB_0, while adding the required driving capacity.

(a) Using a CPU accumulator register A with 'ldaa' (load accumulator A) and 'staa' (store accumulator A) instructions available, write a sequence of assembly instructions to display the number '8' on the seven-segment display #0.

Port B and Port D are memory mapped with addresses $1004 and $1008, respectively.

(b) Describe a way through which we can observe not just one digit lit as in part (a) above but all digits simultaneously showing '12.05.18' on the display arrangement shown in Figure 6.1. Include the sequence of steps to accomplish this as well as the bit patterns needed for Port B.

No need to include assembly instructions in part (b) just the algorithmic sequence.

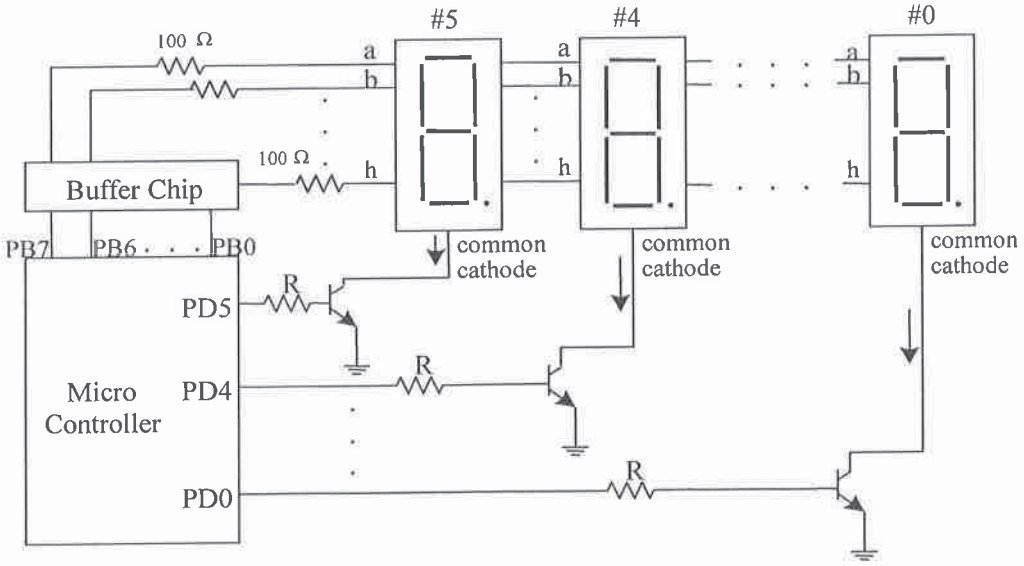


Fig 6.1. Port B and Port D together drive six seven-segment displays

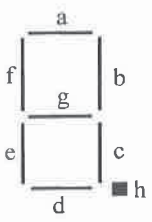


Fig 6.2. Seven-segment display

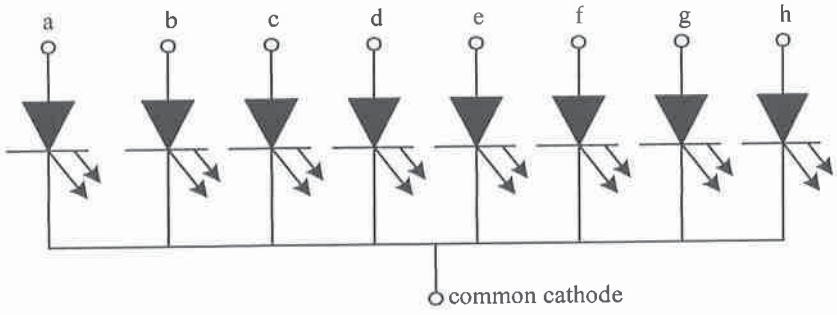


Fig 6.3. Common-cathode seven-segment display

Excitation Table

Q	Q+	R	S	J	K	T	D
0	0	X	0	0	X	0	0
0	1	0	1	1	X	1	1
1	0	1	0	X	1	1	0
1	1	0	X	X	0	0	1

Basic Boolean Identities

	Identity	Comments
1.	$A+0=A$	Operations with 0 and 1
2.	$A+1=1$	Operations with 0 and 1
3.	$A+A=A$	Idompotent
4.	$A+\overline{A}=1$	Complementarity
5.	$A\cdot 0=0$	Operations with 0 and 1
6.	$A\cdot 1=A$	Operations with 0 and 1
7.	$A\cdot A=A$	Idompotent
8.	$A\cdot \overline{A}=0$	Complementarity
9.	$\overline{\overline{A}}=A$	Involution
10.	$A+B=B+A$	Commutative
11.	$A\cdot B=B\cdot A$	Commutative
12.	$A+(B+C)=(A+B)+C=A+B+C$	Associative
13.	$A\cdot(B\cdot C)=(A\cdot B)\cdot C=A\cdot B\cdot C$	Associative
14.	$A\cdot(B+C)=(A\cdot B)+(A\cdot C)$	Distributive
15.	$A+(B\cdot C)=(A+B)\cdot(A+C)$	Distributive
16.	$A+(A\cdot B)=A$	Absorption
17.	$A\cdot(A+B)=A$	Absorption
18.	$(A\cdot B)+(\overline{A}\cdot C)+(B\cdot C)=(A\cdot B)+(\overline{A}\cdot C)$	Consensus
19.	$\overline{A+B+C+\ldots}=\overline{A}\cdot\overline{B}\cdot\overline{C}\cdot\ldots$	De Morgan
20.	$\overline{A\cdot B\cdot C\cdot\ldots}=\overline{A}+\overline{B}+\overline{C}+\ldots$	De Morgan
21.	$(A+\overline{B})\cdot B=A\cdot B$	Simplification
22.	$(A\cdot\overline{B})+B=A+B$	Simplification