National Exams December 2016

98-Comp-A1, Electronics

3 hours duration

NOTES:

1. If doubt exists as to the interpretation of any question, the candidate is urged to indicate, with the answer, a clear statement of any assumptions made.

2. This is a OPEN BOOK exam.
   Any non-communicating calculator is permitted.

3. FIVE (5) questions constitute a complete exam paper.
   The first 5 questions as they appear in the answer book will be marked.

4. Each question is of equal value.

Question 1 (20 marks)

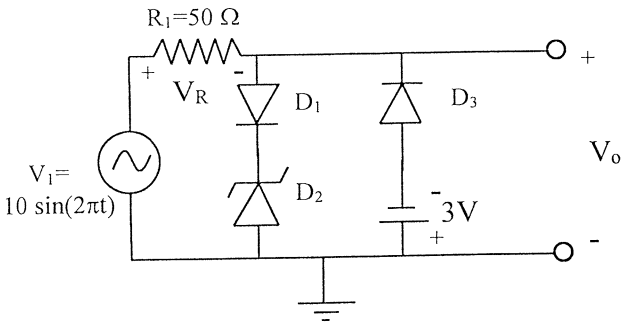

Figure 1. All diodes have a forward voltage drop V_D=0.7V. Diode D_2 has a maximum reverse voltage of 4.3V.

The circuit shown in Figure 1 is in steady state:

a) Sketch V_1 and V_o as a function of time, indicating peak voltages.
b) Sketch V_R, as a function of time, indicating peak voltages.
c) What is the peak current through R_1?
d) Which diode has the largest peak power dissipation? What power rating would you choose for this diode?

Question 2 (20 marks)

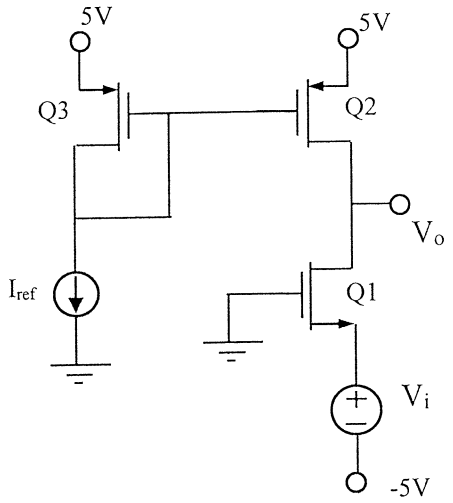

Figure 2. I_{ref}=100 μA, $k_n'=\mu_n C_{ox}$=100 μA/V^2, k_p'=50 μA/V^2, W/L=50, $|V_t|$=1V, V_A=50V and χ=0.2. (W/L)=5 for all transistors.

For the circuit shown in Figure 2:

a) Draw a small signal equivalent model for the circuit.
b) Find the input resistance of the circuit.
c) What is the small signal AC voltage gain of the circuit?

Question 3 (20 marks)

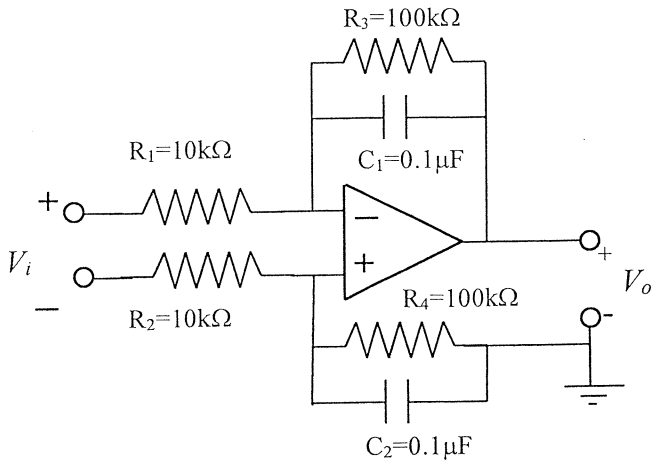

Figure 3.

For the circuit shown in Figure 3:

a) Find the circuit DC gain.
b) Find the circuit AC gain.
c) Sketch the frequency response, indicating 3dB frequencies for this circuit.
d) If the op-amp output is limited by the supply to +/-15V, and $V_i(t)$=Asin(120πt) V, find a maximum value of A such that $V_o(t)$ is not clipped or distorted..

Question 4(20 marks)

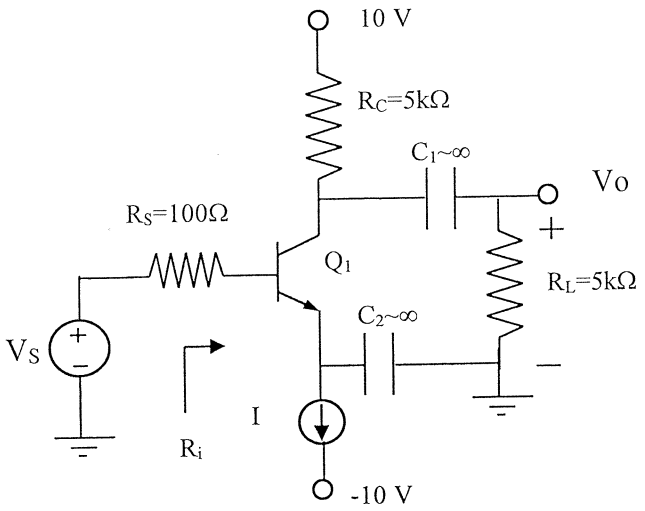

Figure 4. I=0.2mA, β=100, V_A=100V.

For the circuit shown in Figure 4:

a) Draw the small signal equivalent circuit.

b) Find the small signal input resistance R_i and output resistance Ro.

c) Find the open circuit voltage gain for the amplifier and the loaded voltage gain.

Question 5 (20 marks)

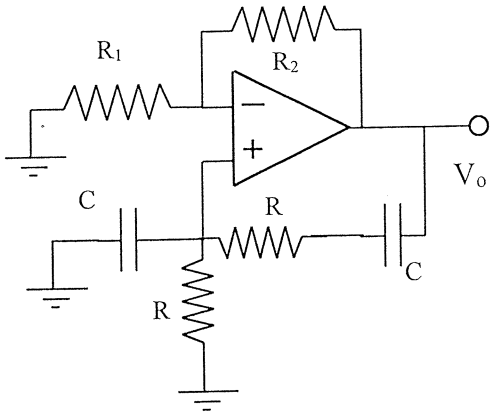

Figure 5. R=10kΩ, C=0.1μF

For the circuit shown in Figure 5:

a) What is the condition for oscillation of the output?

b) What are the frequency and amplitude of the output signal?

c) Choose component values R_1 and R_2 to sustain oscillation.

Question 6 (20 marks)

Consider a CMOS inverter with parameters $k_n' = \mu_n C_{ox} = 100\ \mu A/V^2$, $k_p' = 50\ \mu A/V^2$, $|V_t| = 1V$, $V_{DD} = 5V$.

a) Synthesize a CMOS logic circuit that will realize the Boolean function $F = \overline{D + A \cdot (B + C)}$.

b) An inverter in this technology with a minimum gate length L=0.5 μm has a symmetric transfer function for NMOS W/L = 2 and PMOS W/L = 5. Choose sizes for the transistors in the gate design from a) in order to maintain a symmetric characteristic.

c) If the gate must drive a capacitance of 1pF, estimate the propagation delay for this circuit?

Question 7 (20 marks)

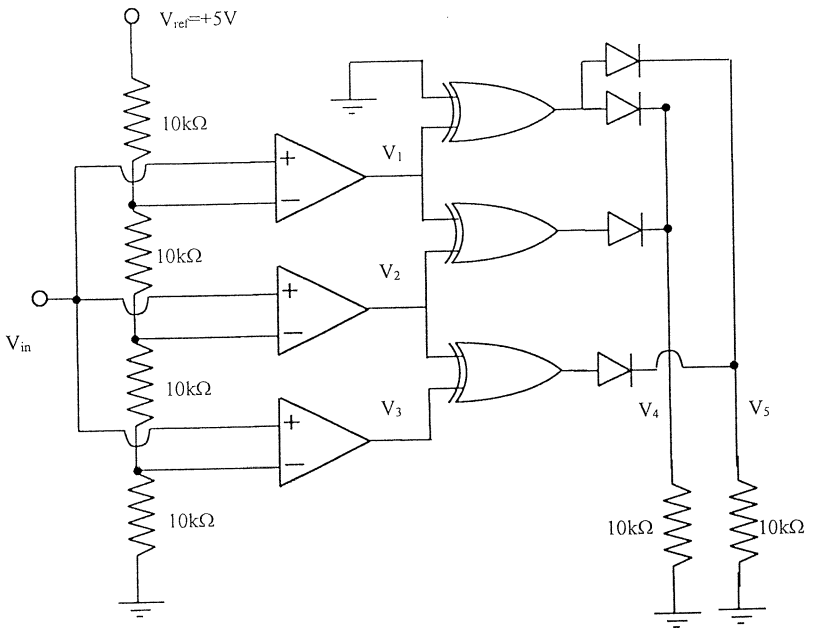

Figure 6.

a) Write expressions relating V_1, V_2, and V_3 to V_{in}.

b) Write expressions relating V_4 and V_5 to V_1, V_2, and V_3.

c) If 4 output bits are needed, how many comparators would be required?

d) What is the resolution (in volts) of this circuit?

Marking Scheme

1. 20 marks total (4 parts, 5 marks each)
2. 20 marks total (a. 7 marks, b. 5 marks, c. 8 marks)
3. 20 marks total (4 parts, 5 marks each)
4. 20 marks total (a. 7 marks, b. 6 marks, c. 7 marks)
5. 20 marks total (a. 10 marks, b. 5 marks, c. 5 marks)
6. 20 marks total (a. 7 marks, b. 6 marks, c. 7 marks)
7. 20 marks total (4 parts, 5 marks each)