National Exams December 2015

98-Comp-A3, Computer Architecture

3 hours duration

NOTES:

1. If doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumptions made.

2. This is a **CLOSED BOOK EXAM.**
   Any non-communicating calculator is permitted.

3. FIVE (5) questions constitute a complete exam paper.
   The first five questions as they appear in the answer book will be marked.

4. Each question is of equal value.

5. Most questions require an answer in essay format. Clarity and organization of the answer are important.

Marking Scheme

1. (a) 5 marks (b) 5 marks (c) 10 marks
2. (a) 5 marks (b) 5 marks (c) 10 marks
3. (a) 5 marks (b) 5 marks (c) 10 marks
4. (a) 5 marks (b) 5 marks (c) 10 marks
5. (a) 5 marks (b) 5 marks (c) 5 marks (d) 5 marks
6. (a) 5 marks (b) 5 marks (c) 10 marks

Question 1: (Total: 20 marks)

(a) (5 marks)
Do you agree or disagree with the following statement: "The bigger the cache size the better the system's performance". JUSTIFY your answer.

(b) (5 marks)
In designing a control unit, discuss the advantages and disadvantages of:
(1) Horizontal micro-instructions.
(2) Vertical micro-instructions.

(c) (10 marks)
Consider a 64-bit microprocessor, a 32-bit microprocessor, and a 16-bit microprocessor. Assume that all processors have bus cycles with the same duration. Assuming that, on average, 25% of the operands and instructions are 64 bits long, 45% are 32 bits long, 20% are 16 bits long, and 10% are 8 bits long. Calculate the relative performance of the three processors when fetching instructions and operands.

Question 2: (Total: 20 marks)

(a) (5 marks)
Once the cache has been filled, when a new block is brought into the cache, one of the existing blocks must be replaced. Explain 4 common replacement algorithms.

(b) (5 marks)
List and briefly define three techniques for performing I/O (from 3 to 4 sentences for each technique).

(c) (10 marks)
Describe the basic principles for RISC design.

Question 3: (Total: 20 marks)

(a) (5 marks)
When a block is updated in the cache, how to ensure consistency between data in main memory and cache?

(b) (5 marks)
What are the pros and cons of fixed-length and variable-length instruction encodings?

(c) (10 marks)
Draw a block diagram of the hardware implementation of unsigned binary multiplication. Explain the algorithm using a flowchart.

Question 4: (Total: 20 marks)

(a) (5 marks)
Compare between dynamic and static RAM

(b) (5 marks)
The IEEE 32-bit floating-point format uses a sign bit *S*, an 8-bit exponent *E*, and a 23-bit mantissa *M*. What is the equivalent decimal value for:
(3) 1 10000011 11000000000000000000000
(4) 0 10000000 00000000000000000000000

(c) (10 marks)
A given processor has 48 registers, uses 16-bit immediates, and has 191 instructions in its ISA. In a given program, 20% of the instructions take one input register and have one output register, 30% have two input registers and one output register, 25% have one input register, one output register, and take an immediate input as well, and the remaining 25% have one immediate input and one output register.
(1) For each of the four types of instructions, how many bits are required? Assume that the ISA requires that all instructions be a multiple of 8 bits in length.
(2) How much less memory does the program take up if a variable-length instruction set encoding is used as opposed to a fixed-length encoding?

Question 5: (Total: 20 marks)

(a) (5 marks)
In a two-level memory hierarchy (cache + main memory), if the top level has an access time of 8ns and the bottom level has an access time of 60ns, what is the hit rate in the top level required to give an average access time of 10ns?

(b) (5 marks)
Convert the following formula from infix to reverse Polish:
(1) (A+B)×(C+D)+E
(2) (A-B)×(((C-D×E)/F)/G)×H

(c) (5 marks)
Explain the advantages and disadvantages of:
(1) Hardwired control unit
(2) Micro-programmed control unit

(d) (5 marks)
List three factors that influence the micro-program word length in a micro-programmed control unit.

Question 6: (Total: 20 marks)

(a) (5 marks)
Discuss the advantages and disadvantages of storing programs and data in the same memory.

(b) (5 marks)
Describe (briefly) how the following addressing modes work. Explain their advantages and disadvantages
(1) Immediate addressing
(2) Direct addressing
(3) Register addressing
(4) Register indirect addressing

(c) (10 marks)
List a sequence of micro-operations that can implement each of the following:
(1) The fetch cycle.
(2) *ADD R1,X*
// add the contents of memory location *X* to Register *R1*, save result in Register *R1*
(3) *ISZ X*
//Increment and skip if zero: the content of x is incremented by 1. If the result //is 0, the next instruction is skipped.

Consider the notation:
IR= instruction register
MAR = memory address register
MBR = memory buffer register
PC = program counter
C(X) = content of *X* (*X* = register or memory location)