National Exams December 2015

04-BS-8, Digital Logic Circuits

3 hours duration

NOTES:

1. If a doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumptions made with the answer of the question.

2. Candidates may use one of two calculators, the Casio or Sharp approved models. This is a closed book examination; however, candidates are allowed to bring one hand-written information sheet (8.5" X 11") of self-prepared notes.

3. This paper contains **FIVE (5)** questions and comprises **Six (6)** pages.

4. Any **FOUR (4)** questions constitute a complete paper. Only the first four questions as they appear in your answer book will be marked.

5. All questions are of equal marks. Total marks = 100

6. Each question carries 25 marks and the marks for each part of the questions are indicated in brackets.

7. A PAL16L8 Data sheet is provided in the Appendix. It can be used to provide the solution of Question 2, part (b) and should be attached to your answer sheet.

1. A digital system is to be developed that can monitor the available parking spaces in a 220-space parking garage with one entrance and two exit gates. The circuit provides an indication of full garage by illuminating a FULL display sign and lowering the entrance gate bar. Salient features of the system are:
   - A sensor at the entrance gate produces a positive TTL pulse when a vehicle enters the garage via that gate.
   - One sensor at each exit gate produces a positive TTL pulse when a vehicle leaves the garage from either of the exit gates.
   - The sequential circuit counts up when a vehicle enters and counts down when the vehicle leaves the garage.
   - The circuit produces a HIGH TTL output when the garage is full. This HIGH output signal is used to illuminate the Full sign and to close the vehicle entrance gate of garage.
   - The circuit output changes to LOW when an empty space becomes available in the garage.

   Design and implement the digital circuit using a suitable size up/down counters (e.g. 74193) and some other logic gates.

   (a) Show your complete design with full details including the up/down counter and other logic gates.

   (17 marks)

   (b) Briefly describe the working operation of your designed circuit.

   (8 marks)

2. (a) Define a 3-bit Gray code and identify at least one advantage of employing Gray codes in digital circuits.

   (5 marks)

   (b) Show the AND/OR connections required to implement a 3-bit Gray code to binary coded decimal (BCD) conversion. Complete the PAL16L8 programmable logic diagram in the Appendix and attach it to your answer book.

   (12 marks)

   (c) Implement the same 3-bit Gray code to BCD conversion circuit of part (b) by using a 3-to-8 decoder with minimum number of gates.

   (8 marks)

3. Braille is a system of raised dots that can be read by a blind person. The Braille patterns for the numbers 0-9 are shown in Figure Q3. Design a digital system that converts binary coded decimal (BCD) numbers to Braille.

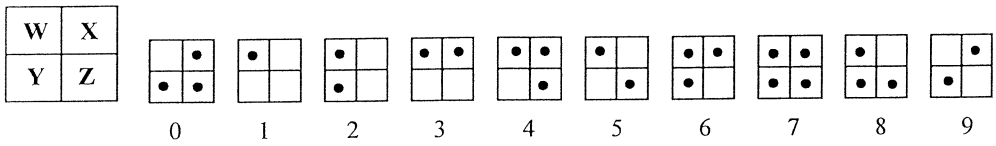


Figure Q3

(a) Derive the minimized sum-of-products (SOP) equation for each of the four Braille dot outputs (W, X, Y, and Z) given a 4-bit BCD number (B_3 B_2 B_1 B_0) as input. The BCD inputs and the Braille dot outputs are active-HIGH. List any assumptions that you may have made.

(13 marks)

(b) Implement the minimized Boolean expression for Y using only 2-input NOR gates.

(7 marks)

(c) Implement the expression for W by using minimum number of gates.

(5 marks)

4. Design a clocked synchronous finite state machine (FSM) with three inputs, RESET, ENABLE and SERIAL_DATA, and two outputs, EVEN and ODD.
   - The RESET input clears the state memory to 0. The ENABLE input allows the circuit to operate.
   - The SERIAL_DATA input has 0s and 1s in a random order. The SERIAL_DATA input is synchronized to the CLOCK such that t_{SETUP} and t_{HOLD} are always satisfied (i.e. SERIAL_DATA does not change on a CLOCK edge).
   - The EVEN output is asserted (1) if the number of 1s since RESET is even. The ODD output is asserted (1) if the number of 1s since RESET is odd.

Question #4 continues on Page 4

(a) Draw the state diagram and table of the required finite state machine.

(10 marks)

(b) Design and implement the finite state machine circuit by using the minimum number of D-type flip-flops and basic logic gates. Show your complete design with full details including simplification of next state equations and the finite state machine circuit.

(15 marks)

5. (a) Show how a J-K flip-flop can be constructed by using a T (toggle) flip-flop and other logic gates. Draw the complete logic diagram of the circuit.

(6 marks)

(b) Design and draw a sequential circuit using an edge-triggered S-R flip-flop that produces an 8MHz frequency signal with 50% duty cycle from a 16MHz clock signal with 20% duty cycle.

(7 marks)

(c) A sequential circuit containing an eight-bit shift register is shown in Figure Q5. Initially, the shift register is loaded with $(01101010)_2$ and the J-K flip-flop is cleared. Determine the content of the shift register after eight clock pulses have been applied. You may ignore any propagation delays.

(12 marks)

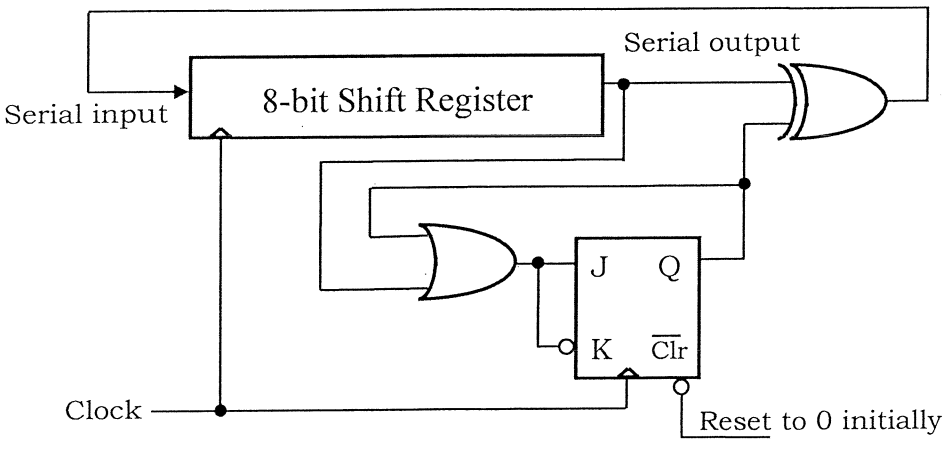
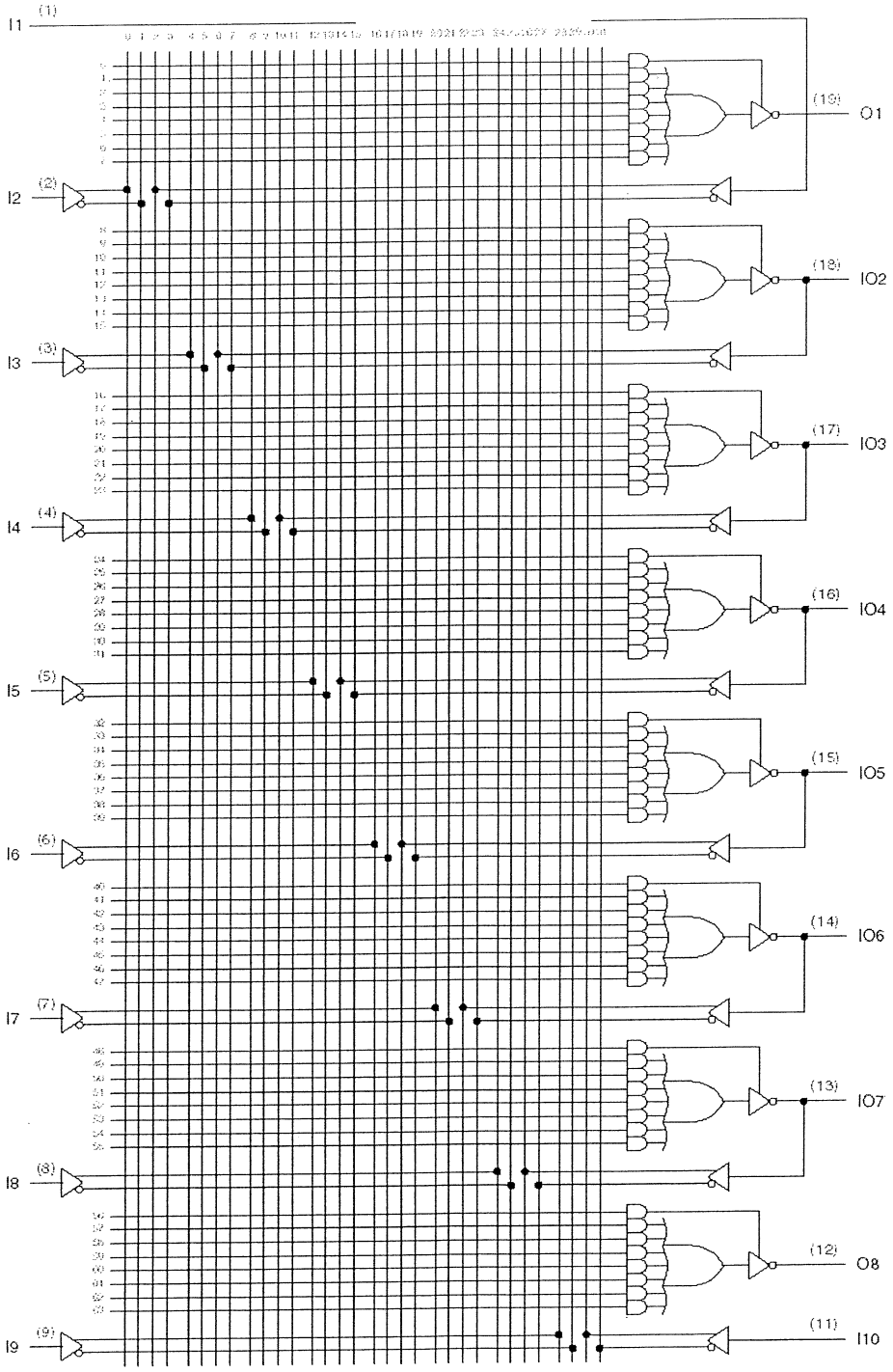


Figure Q5

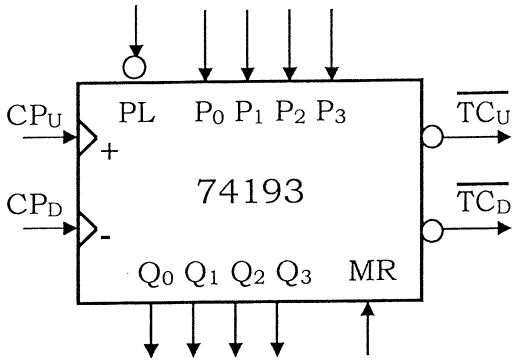
APPENDIX
PAL16L8



Counter and Decoder Data Sheets

74193, 4-bit UP/DOWN Counter

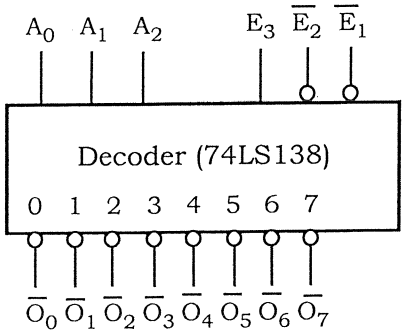
MR	$\overline{PL}$	CP_U	CP_D		Mode
H	x	x	x		Asynch reset
L	L	x	x		Asynch Load
L	H	H	H		No change
L	H	↑	H		Count up
L	H	H	↑		Count down



Pins	Description
CP_U	Count-up clock input
CP_D	Count-down clock input
MR	Asynchronous master reset input
$\overline{PL}$	Asynchronous parallel load input
P_0-P_3	Parallel data inputs
Q_0-Q_3	Flip-flop outputs
$\overline{TC_U}$	Terminal count-up (carry) output
$\overline{TC_D}$	Terminal count-down (borrow) output

74LS138: 3-to-8 Decoder

Inputs			
$\overline{E_1}$	$\overline{E_2}$	E_3	
0	0	1	Respond to input code $A_2A_1A_0$
1	x	x	Disabled all HIGH
x	1	x	Disabled all HIGH
x	x	0	Disabled all HIGH



End of Paper

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Marking Scheme

1. 25 Marks Total
   (a) 17 marks
   (b) 8 marks

2. 25 Marks Total
   (a) 5 marks
   (b) 12 marks
   (c) 8 marks

3. 25 Marks Total
   (a) 13 marks
   (b) 7 marks
   (c) 5 marks

4. 25 Marks Total
   (a) 10 marks
   (b) 15 marks

5. 25 Marks
   (a) 6 marks
   (b) 7 marks
   (c) 12 marks