National Exams December 2014

04-BS-8, Digital Logic Circuits

3 hours duration

NOTES:

1. If a doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumption made with the answer of the question.

2. Candidates may use one of two calculators, the Casio or Sharp approved models. This is a closed book examination; however, candidates are allowed to bring the following into the examination room:

    (i) One hand-written information sheet (8.5" X 11") of self-prepared notes.

3. This paper contains **FIVE (5)** questions and comprises **FIVE (5)** pages.

4. Any **FOUR (4)** questions constitute a complete paper. Only the first four questions as they appear in your answer book will be marked.

5. All questions are of equal marks. Total marks = 100

6. Each question carries 25 marks and the marks for each part of questions are indicated in brackets.

7. A PAL16L8 Data sheet is provided in the Appendix. It can be used to provide the solution of Problem 2, part (b) and should be attached to your answer sheet.

1. (a) Identify any advantages and disadvantages of BCD and Gray codes.

(6 marks)

(a) Design a combinational logic circuit that converts 4-bit Gray codes to Binary numbers. Construct the truth table and produce simplified Boolean expressions using K-maps. Implement the Boolean expressions with the minimum number of logic gates.

(13 marks)

(b) Implement the combinational logic circuit developed in part (a) by using minimum number of 2-input NAND gates.

(6 marks)

2. (a) Identify the main differences between PAL and FPGA devices.

(6 marks)

(b) Implement the following Boolean expression by using a PAL16L8 programmable logic device.

$$F(a, b, c, d) = \sum m(0, 2, 4, 6, 7, 9, 11, 13)$$

Attach the duly completed PAL16L8 diagram to your answer book.

(7 marks)

(c) ALM (Adaptive Logic Module) or CLB (Configurable Logic Block) are the basic logic blocks of FPGAs produced by Altera or Xilinx. Identify the main components of an FPGA logic block. You may like to draw a rough block diagram of ALM or CLB used in FPGAs.

(12 marks)

3. Design a finite state machine with two inputs (**x** and **y**) and one output, **z**. The state table of the finite state machine is given below.

Present State	Next State xy= 00	01	10	11	Output Z
A	B	A	B	C	1
B	D	C	B	A	1
C	B	C	A	D	0
D	B	C	D	A	1

(a) Draw the state diagram and determine the number of flip-flops required to implement the finite state sequential machine. Justify your answers.

(8 marks)

(b) Use D-type flip-flops and other logic gates to design the above finite state machine. Show the full details of your design.

(17 marks)

4. (a) Show how a D-type flip-flop can be constructed by using a JK flip-flop and other logic gates. Draw the complete logic diagram of the circuit.

(6 marks)

(b) Design and implement a 4-bit counter that counts down in sequence (---- 15, 13, 11, 9, 7, 5, 3, 1, 15 -----) by using the minimum number of D-type flip flops and basic logic gates. Show your complete design.

(19 marks)

5. Design and implement a Combinational Logic Circuit to generate parity for a 7-bit data. The value of an odd parity is chosen so that the total number of 1s in the coded 8-bit data (including the parity bit) is an odd number. Similarly the even parity bit is chosen so that the total number of 1s in the coded data group (including the parity bit) is an even number.

The combinational logic circuit block that generates either odd or even parity depending on a control input EP is shown in Figure Q5. The circuit should generate an even parity when EP = 1 and an odd parity when EP = 0. The parity generator has a parallel data input $D_0, D_1, D_2, ----- D_6$.

(a) Show your full design by drawing the fully operational circuit with minimum of logic gates.
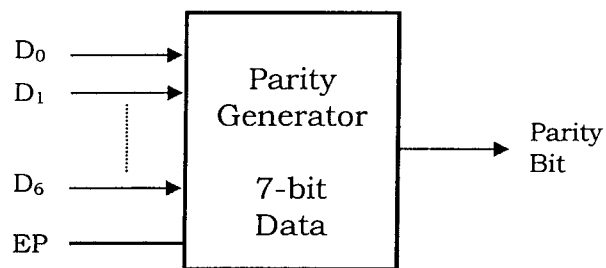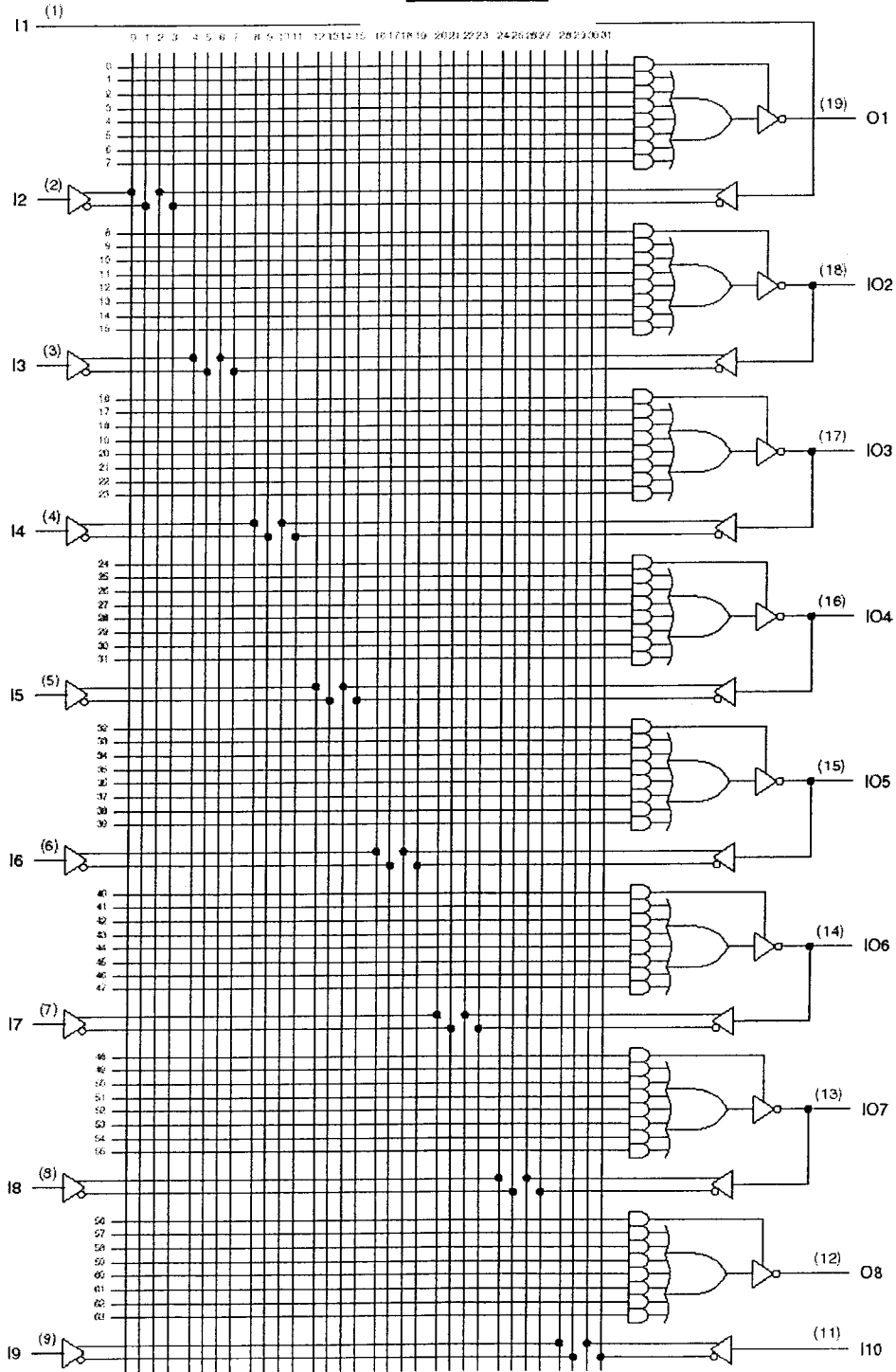
(16 marks)

Figure Q5

(b) Suggest any modification in the parity generator circuit of part (a) so that the circuit can be used for checking the parity of an incoming 7-bit datum along with its parity.

(9 marks)

APPENDIX
PAL16L8

End of Paper

Marking Scheme

1. 25 Marks Total
    (a)   6 marks
    (b)   13 marks
    (c)   6 marks

2. 25 Marks Total
    (a) 6 marks
    (b) 7 marks
    (c) 12 marks

3. 25 Marks Total
    (a)   8 marks
    (b)   17 marks

4. 25 Marks Total
    (a)   6 marks
    (b)   19 marks

5. 25 Marks
    (a) 16 marks
    (b) 9 marks