National Exams December 2018

17-Comp-A1, Electronics

3 hours duration

NOTES:

1. If doubt exists as to the interpretation of any question, the candidate is urged to indicate, with the answer, a clear statement of any assumptions made.

2. This is an OPEN BOOK exam.
   Any non-communicating calculator is permitted.

3. FIVE (5) questions constitute a complete exam paper.
   The first 5 questions as they appear in the answer book will be marked.

4. Each question is of equal value.

Marking Scheme

1. 20 marks total (4 parts, 5 marks each)
2. 20 marks total (4 parts, 5 marks each)
3. 20 marks total (4 parts, 5 marks each)
4. 20 marks total (4 parts, 5 marks each)
5. 20 marks total (4 parts, 5 marks each)
6. 20 marks total (4 parts, 5 marks each)
7. 20 marks total (4 parts, 5 marks each)

Question 1 (20 marks)

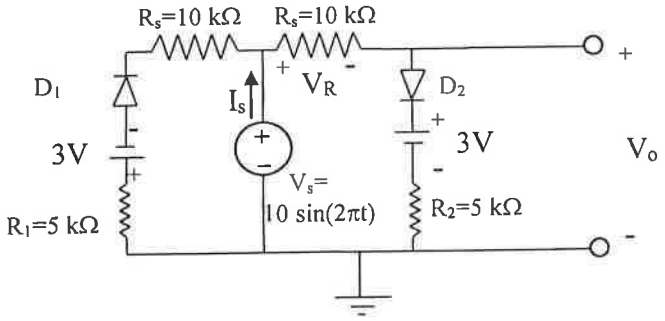

Figure 1. All diodes have a forward voltage drop V_D=0.7V.

The circuit shown in Figure 1 is in steady state:

a) Sketch V_s and V_o as a function of time, indicating peak voltages.
b) Sketch V_R, as a function of time, indicating peak voltages.
c) Which resistor has the largest peak power dissipation? What power rating would you choose for this resistor?
d) Sketch current I_s as a function of time, indicating peak values.

Question 2 (20 marks)

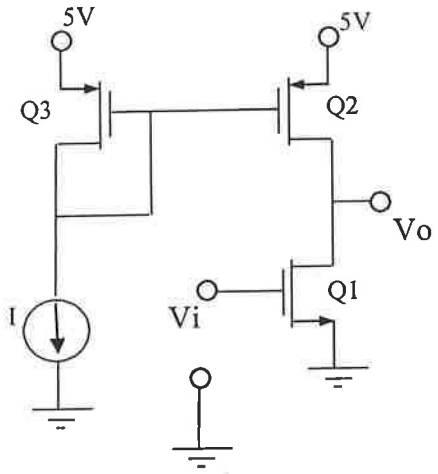

Figure 2. I=500 μA, $k_n'(W/L)=3k_p'(W/L)=1$ mA/V^2, $V_{tn}=|V_{tp}|=1.0$V, $V_A=80$V

For the circuit shown in Figure 2:

a) Draw a small signal AC equivalent circuit and find the model parameter values.
b) Find the input and output resistances of the circuit.
c) Find the open circuit voltage gain for the amplifier.
d) If the output drives a 50Ω load, what is the voltage gain?

Question 3 (20 marks)

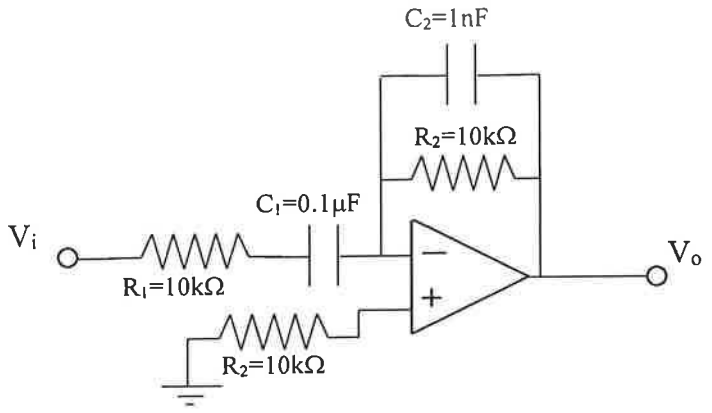

Figure 3. The operational amplifier saturates at +/- 10V. The DC input bias current in each input terminal is 10 μA.

For the circuit shown in Figure 3:

a) Find the circuit AC gain.
b) Sketch the frequency response of the circuit.
c) Find the 3dB frequencies, bandwidth and passband gain for this circuit.
d) What is the effect of the input bias current on output voltage offset?

Question 4(20 marks)

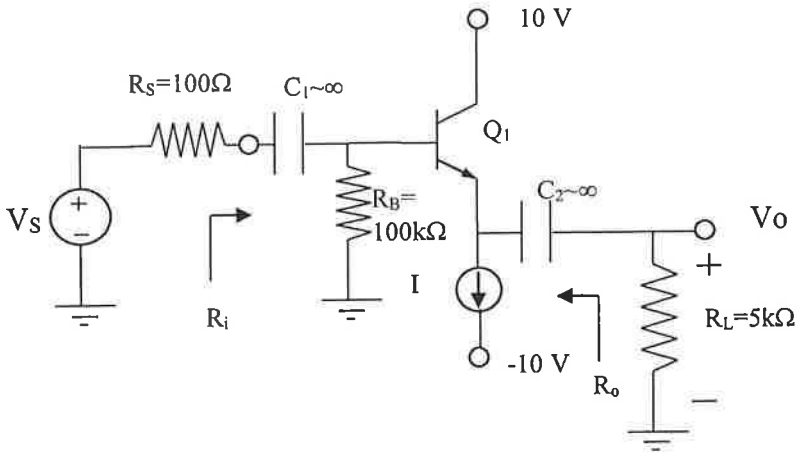

Figure 4. I=1mA, β=100, V_A=100V, V_T=25mV.

For the circuit shown in Figure 4:

a) Find V_C, V_B and V_E.
b) Draw a small signal equivalent circuit and find the model parameter values.
c) Find the small signal input resistance R_i and output resistance Ro.
d) Find the open circuit voltage gain for the amplifier and the loaded voltage gain.

Question 5 (20 marks)

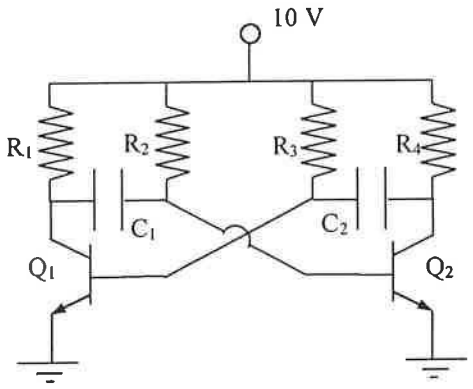

Figure 5. $R_1=R_4=1k\Omega$, $R_2=R_3=10k\Omega$, $C_1=C_2=1nF$

For the circuit shown in Figure 5:

a) Explain operation of the circuit.
b) Where would you take the circuit output?.
c) For the component values given, at what frequency would the circuit operate ?
d) Select new component values to provide a duty cycle of 66% at the same operating frequency.

Question 6 (20 marks)

Consider a CMOS technology in which an inverter with a minimum gate length L=0.5 μm has a symmetric transfer function for NMOS W/L = 1.5 and PMOS W/L =6.

a) Sketch the transistor level gate schematic for the Boolean function $Y = \overline{(AB + C)D}$.
b) Specify sizes (W/L) for all transistors in order to achieve current-driving capability equal to that of the basic inverter.
c) Repeat a) and b) $Y = A\overline{B} + \overline{A}B$.
d) For the gate in c), find the ratio of maximum to minimum available current to charge and discharge a load.

Question 7 (20 marks)

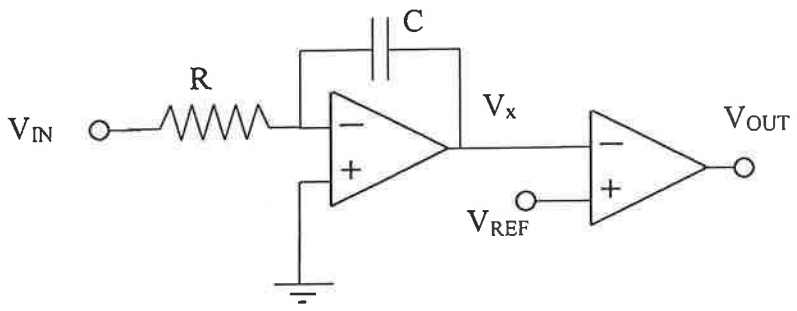

Figure 6. V_{REF} is a positive reference. The capacitor is initially discharged. $R=10k\Omega$, $C=10\mu F$, $V_{IN}=-2V$, $V_{REF}=2.5V$

a) For a DC input V_{IN}, sketch $V_x(t)$.

b) Find the slope of $V_x(t)$.

c) A counter with a clock of 1MHz stops when V_{OUT} goes high. What is the counter value?

d) What are the applications and limitations of this circuit?