National Exams May 2019

17-Comp-A2, Digital Systems Design

3 hours duration

NOTES:

1. If doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumptions made.
2. This is a Closed Book exam.
   Candidates may use one of two calculators, the Casio or Sharp approved models.
3. FIVE (5) questions constitute a complete exam.
4. All questions are worth 20 points

Marking Scheme

1. (1.1) 2, (1.2) 2, (1.3) 2, (1.4) 2, (1.5) 2, (1.6) 2, (1.7) 2, (1.8) 2, (1.9) 2, (1.10) 2 total = 20
2. (a) 5, (b) 15, total = 20
3. (a) 5, (b) 5, (c) 5, (d) 5, total = 20
4. (a) 15, (b) 5, total = 20
5. (a) 7, (b) 7, (c) 6, total = 20
6. (a) 4, (b) 4, (c) 4, (d) 4, (e) 4,total = 20

The number beside each part above indicates the points that part is worth

1) Circle the letter of the best answer (20 points)

1.1 The abbreviation RTL means: [2 pts]

A. Relational Timing Logic
B. Relative Transfer Latches
C. Register Transfer Level

1.2 Using true/false values, the two-input xor operator gives true when : [2 pts]

A. both inputs are the same
B. both inputs are different
C. either input is true

1.3 The process statement is one of the: [2 pts]

A. Sequential statements
B. Design units
C. Concurrent statements

1.4 The term sequential means: [2 pts]

A. happening quickly
B. happening over and over
C. happening in steps, one after the other

1.5 Syntax and semantics refer to what two concepts? [2 pts]

A. format and structure
B. grammar and meaning
C. behavior and timing

1.6 Propagation delay is what? [2 pts]

A. The time to flip-flops initialized
B. The time to get input changes to affect outputs
C. The time from one clock edge to the next.

1.7 The process sensitivity list normally contains: [2 pts]

A. Process outputs
B. Process inputs
C. Both process inputs and outputs

1.8 Concurrent execution is done by: [2 pts]

A. Executing when triggered
B. Executing in the order written
C. Executing after a delay

1.9 The following are three sequential statements: [2 pts]

A. Variable assignment; if/then/else;
selected concurrent signal assignment
B. Case; loop; conditional concurrent signal assignment
C. Signal assignment; loop; variable assignment

1.10 Variables are assigned the new value [2 pts]

A. Immediately
B. After a delay
C. When the simulator completes the next cycle

2). Function F is defined by the truth table given below

C \ AB	00	01	11	10
0	0	1	1	0
1	1	0	0	1

a) Write out the expression F in terms of A,B,C [5 pts]
b) Use a 8-to 1 multiplexer to implement the function [15 pts]

3). Given the following function in product of sums form, not necessarily minimized:

$$F(W,X,Y,Z) = (W+\overline{X}+\overline{Y})(\overline{W}+\overline{Z})(W+Y)$$

(a) Express the function in the canonical sum of products form, use "little m" notation. [5 pts]

(b) Re-express the function in the minimized sum of product form. [5 pts]

(c) Express $\overline{F}$ in the minimized sum of product form. [5 pts]

(d) Re-express $\overline{F}$ in the minimized product of sum form. [5 pts]

4). A circuit is needed to start and stop counting clock pulses on command.

(a) Design a 3-bit synchronous counter that goes through the sequence 000, 001, 010, 011, 100, 101, 110, 111 and then repeats. Use positive-edge-triggered JK flip-flops. Label the bits Q_C, Q_B & Q_A where Q_C is the most significant bit. Draw the circuit implementing the counter. [15 pts]

(b) Modify the circuit so that it counts whenever an additional COUNT ENABLE (CTE) input is HIGH, stops counting when CTE goes LOW and resumes counting from where it stopped when CTE goes HIGH again. [5 pts]

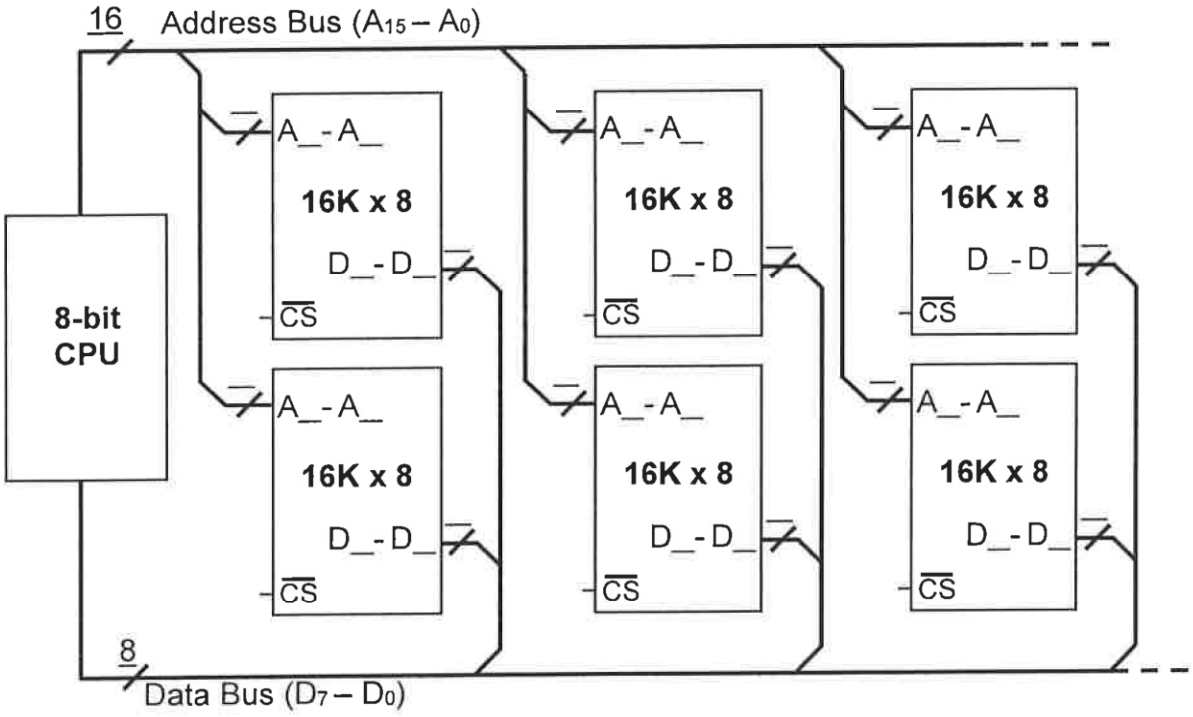
5). Provide this 8-bit CPU with a 64Kbyte memory space by making use of 16K x 4 memory chips like the ones provided in the figure below.

(a) Fill in the blanks *beside* and *inside* the memory chips with the appropriate numbers. The number on top of this symbol —/— represents the number of lines on that bus. The spaces besides the A's and the D's are to indicate which lines of the address and data busses are connected to each chip, respectively. [7 pts]

(b) Complete the connections in the figure below adding logic gates where needed to produce the chip select ($\overline{CS}$) signals needed in the decoding logic. Explain the reasons for the connections made, include expressions for the Boolean logic used. [7 pts]

(c) Provide the address range allocated to each of the chips used. [6 pts]

Note: R/$\overline{W}$ & clock signals are omitted for simplicity.



6).

A) What is the name given to a routine that is executed in response to an interrupt? [4 pts]

B) What are the advantages of using interrupts to handle data inputs and output? [4 pts]

C) What are the requirements of interrupt processing? [4 pts]

D) How do you enable other interrupts when the controller is executing an interrupt service routine? [4 pts]

E) Why would there be a need to promote one of the maskable interrupts to highest priority among all maskable interrupts? [4 pts]