National Exams May 2014

07-Elec-A5, Electronics

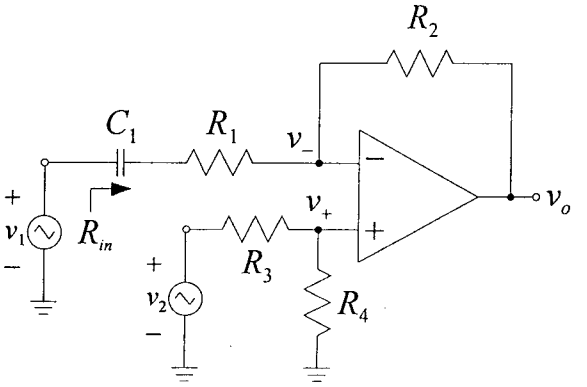
3 hours duration

Notes:

1. If any doubt exists as to the interpretation of any question, the candidate is urged to submit, within their answer, a clear statement of any assumptions made.
2. This is a **CLOSED BOOK EXAM.**
   Any non-communicating calculator is permitted.
3. Answer all **FIVE** (5) questions.
4. All questions are worth 20 marks each.
5. Please start each question on a new page and clearly identify the question number and part number, e.g. Q4(a).
6. In schematics, ground and chassis may be assumed to be common, unless specifically stated otherwise.
7. Unless otherwise specified, assume that Op-Amps are ideal and that supply voltages are ±15V.
8. If questions require an answer in essay format, clarity and organization of the answer are important. Provide block diagrams and circuit schematics whenever necessary.

QUESTION (1)

The op amp in this circuit is ideal except for an input bias current of 100nA in each of the input terminal.



Given $C_1 = \infty$, design this circuit to meet the following specifications:

a) $v_o = v_2 - v_1$
b) $R_{in} = 1\ \text{M}\Omega$
c) Minimum output offset voltage

Provide values for R_1, R_2, R_3 and R_4. (20 points)

QUESTION (2)

The p-channel MOSFET, M_1 in this circuit has the following characteristics:

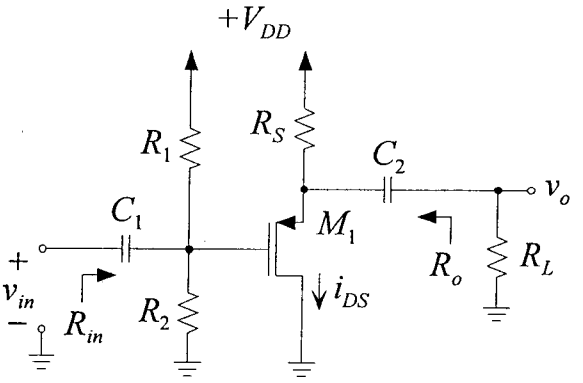
$|V_{TH}| = 1\ \text{V}$

$K = 2\ \text{mA/V}^2$ $\lambda = 0.01\ \text{V}^{-1}$

Given:

$V_{DD} = 10\ \text{V}$ $R_L = R_S = 2\ \text{k}\Omega$

$C_1 = C_2 = \infty$



a) Design this circuit to have the following specifications:
$R_{in} = 100\ \text{k}\Omega$, $I_{SD} = 2\text{mA}$
Provide values for R_1, and R_2. (8 points)

b) Determine the output resistance, R_o. (6 points)

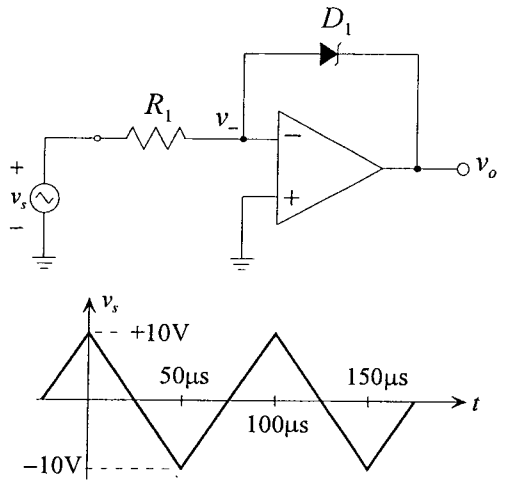
c) Determine the maximum undistorted peak to peak output voltage? (6 points)

Useful formulae: for p-channel MOSFET

$$i_{SD} = K\left[2(v_{SG} - |V_{TH}|)v_{SD} - v_{SD}^2\right] \quad \text{triode region}$$

$$i_{SD} = K\left(v_{SG} - |V_{TH}|\right)^2\left(1 + \lambda v_{SD}\right) \quad \text{saturation region}$$

QUESTION (3)

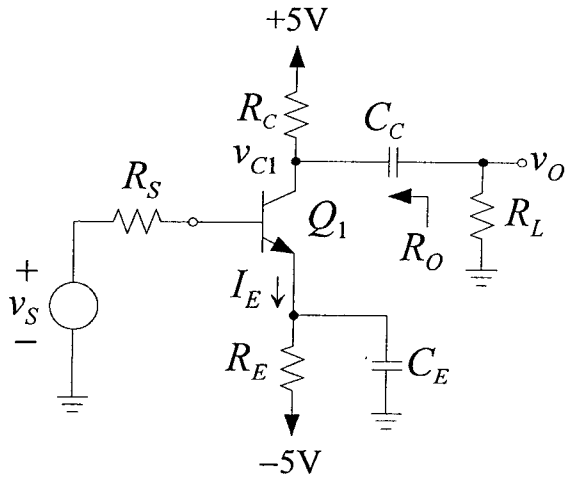


The op amp in this circuit is ideal except for a slew rate limit of 0.5V/μs. It is powered by ±15V supplies. Given that

$R_1 = 10\text{k}\Omega$
For D_1, $V_Z = 5\text{V}$, forward voltage drop = 0.7V

Sketch **accurately** in your answer book the voltage waveform for v_O. You must indicate the breakpoints, including the accurate timing and voltage levels. (20 points)

QUESTION (4)



The BJT, Q_1 has the following characteristics:

$\beta = 100$
$V_{BE(\text{on})} = 0.7\text{V}$
$V_{CE(\text{sat})} = 0.3\text{V}$
$V_A = \infty$
$R_S = 100\Omega$
C_E, and C_C are large capacitors

a) Design this common collector amplifier circuit to have an open circuit gain (i.e. without R_L) of 100V/V with a DC bias current, $I_E = 2\text{mA}$.
Provide values for R_E and R_C. (8 points)

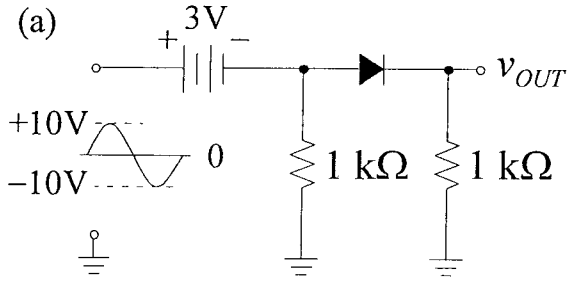
b) What is the equivalent output resistance, R_O? (6 points)

c) For a 1mV peak to peak sine wave input at 1 kHz, sketch accurately the waveforms at the collector of Q_1, v_{C1} and at the output v_O. Remember to take into account the fact that $R_L = 1.25\ \text{k}\Omega$. (6 points)

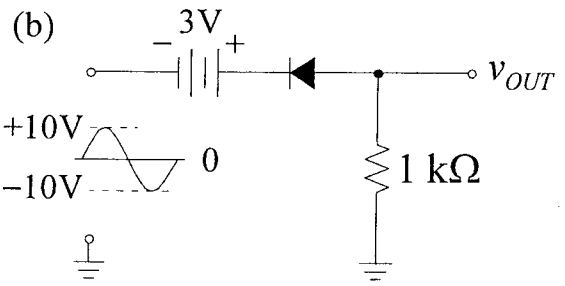
QUESTION (5)

In the following circuits, assume that the diode is ideal and has a forward voltage of 0.7V. Sketch the output waveform for one complete sine wave input. (20 points)

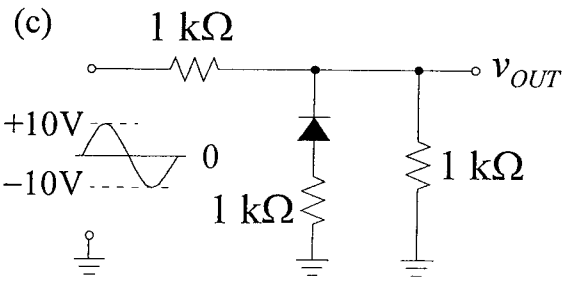
(a)



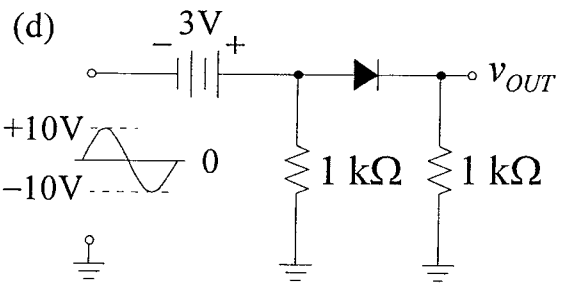
(b)



(c)



(d)



(e)