National Exams May 2019

17-Phys-A5-B Analog and Digital Electronic Circuits

3 hours duration

NOTES:

1. If doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumptions made.

2. This is an OPEN BOOK EXAM.
   Any non-communicating calculator is permitted.

3. Answer all SIX (6) questions.

4. Please start each question on a new page and clearly identify the question number and part number, e.g. Q1(a).

5. If questions require an answer in essay format, clarity and organization of the answer are important. Provide block diagrams and circuit schematics whenever necessary.

Marking Scheme

1. 15 marks
2. (a) 10 marks; (b) 10 marks;
3. (a) 10 marks; (b)10 marks
4. 15 marks
5. (a) 10 marks; (b) 5 marks
6. 15 marks

Question 1

For the circuit, shown in Fig.1, assume the diode has a 0.7 V drop when conducting.

(a) Find the output voltage v_O in terms of the input v_{in} and sketch clearly v_O versus v_{in} when v_{in} changes over the range of ±8V. Mark on the plot the values of v_O for v_{in} =±8V.

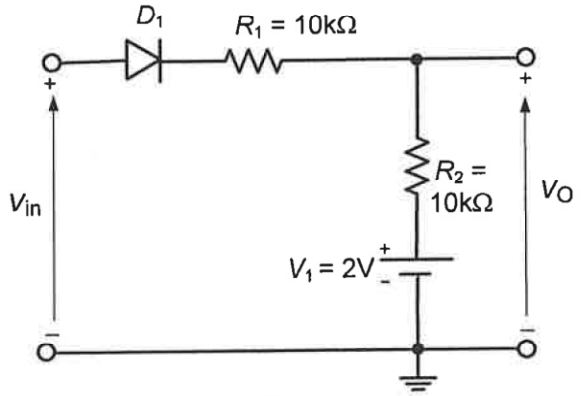

Fig.1

Question2

In the circuit in Fig.2, assume Q_1 has β = 50 and V_{EB} = 0.7V for the dc analysis and neglect Early effect (V_A = ∞).

(a) Find the dc current I_C.

(b) Calculate the input resistance R_i.

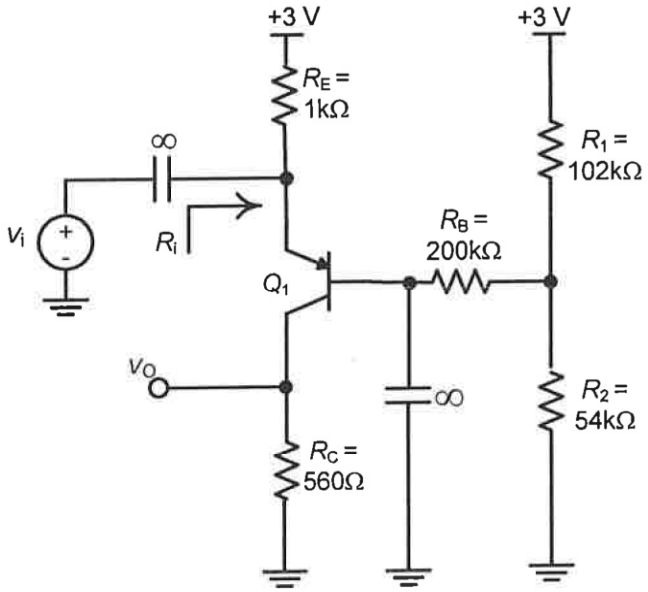

Fig.2

Question3

For the MOS circuit shown in Fig. 3, consider I_{bias} is an ideal current source, V_b is a constant dc voltage, $g_{m1} \neq g_{m2} \neq g_{m3} \neq g_{m4}$, and $r_{o1} \neq r_{o2} \neq r_{o3} \neq r_{o4} \neq \infty$. Assume all the transistors are in active region.

(a) Find the expression of the differential gain $A_d=|v_o/v_{id}|$.
(b) Find the 3-dB frequency, f_H, of the differential gain $A_d=|v_o/v_{id}|$ while including the parasitic capacitances C_{gs} for all transistors.

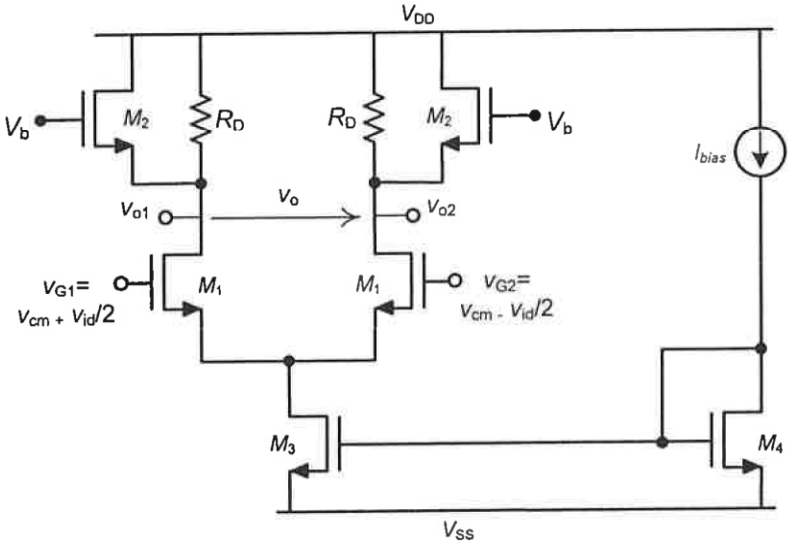

Fig. 3

Question 4

For the amplifier in Fig. 4 assume that $g_{m1} = g_{m2} \neq g_{m3}$, and $r_{o1} = r_{o2} = r_{o3} = \infty$. I_{bias} is an ideal current source. Assume all transistors are in saturation region.

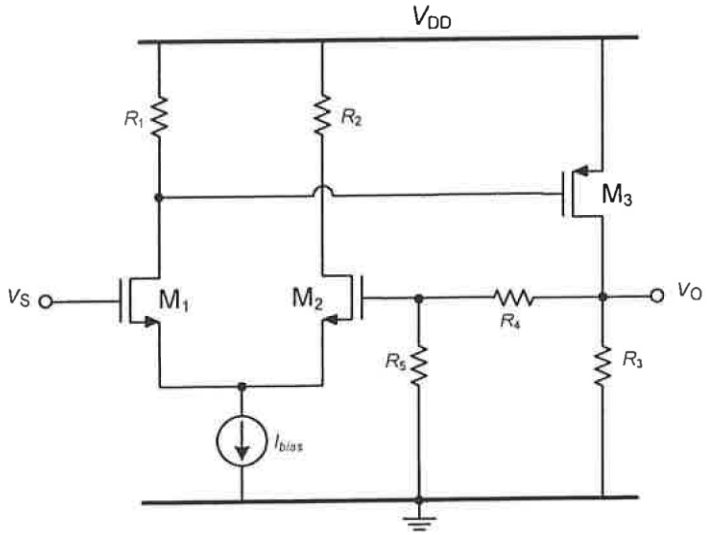

Fig. 4

(a) Use the methods of feedback analysis to find the expression of the gain v_o/v_s.

Question 5

Consider the 3-bit digital-to-analog converter (DAC) using an R-2R resistive ladder as shown in Fig. 5. Assume an ideal Op-Amp.

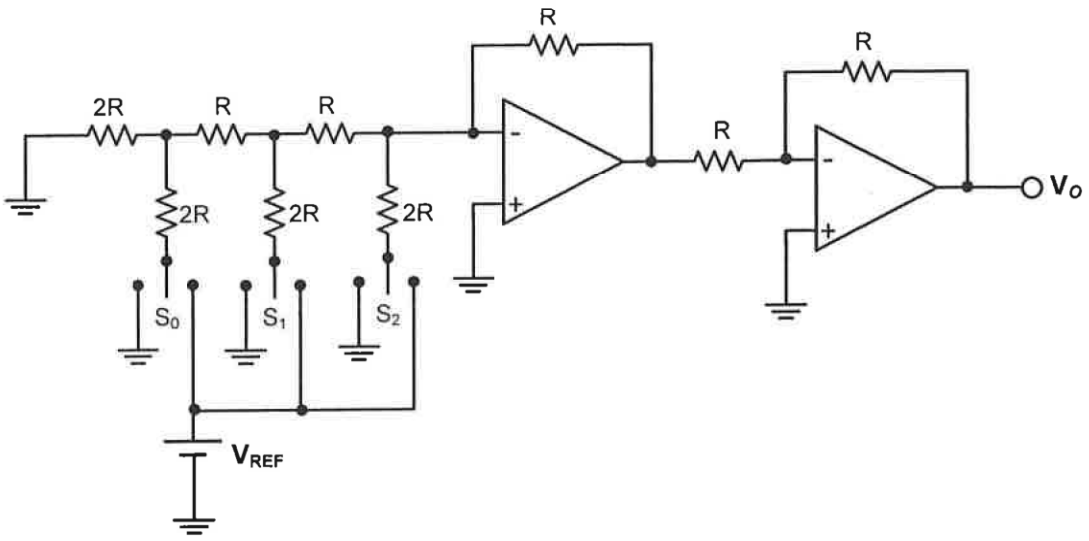

Fig. 5

(a) Find the expressions of the output voltage V_O

(b) Calculate V_O when R = 10kΩ, V_{REF} = 5 V and the applied binary word is $S_2S_1S_0$ =101.

Question 6

Implement the logic function Y = A. B .C + D using static CMOS logic gate with NMOS and PMOS transistors. Mark on the schematic clearly the pull-down network (PDN) and the pull-up network (PUN) that implements the function Y.