National Exams May 2016

98-Comp-A3, Computer Architecture

3 hours duration

NOTES:

1. If doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumptions made.

2. This is a **CLOSED BOOK EXAM**.

   Any non-communicating calculator is permitted.

3. FIVE (5) questions constitute a complete exam paper.

   The first five questions as they appear in the answer book will be marked.

4. Each question is of equal value.

5. Most questions require an answer in essay format. Clarity and organization of the answer are important.

Marking Scheme

1. (a) 5 marks (b) 5 marks (c) 10 marks
2. (a) 5 marks (b) 5 marks (c) 10 marks
3. (a) 5 marks (b) 5 marks (c) 10 marks
4. (a) 5 marks (b) 5 marks (c) 10 marks
5. (a) 5 marks (b) 5 marks (c) 5 marks (d) 5 marks
6. (a) 5 marks (b) 5 marks (c) 5 marks (d) 5 marks

Question 1:   (Total: 20 marks)

(a) (5 marks)
Explain the pros and cons of using a unified cache (store both data and instructions) versus using a split one.

(b) (5 marks)
Identify the inputs to and the outputs from a control unit. Briefly explain the objectives of each signal.

(c) (10 marks)
Consider two microprocessors having 8- and 16-bit-wide external data buses, respectively. The two processors are identical otherwise and their bus cycles take just as long. Assuming that 30% of the operands and instructions are one byte long, and the rest are two bytes long. By what factor do the maximum data transfer rates differ?

Question 2:   (Total: 20 marks)

(a) (5 marks)
Do you agree or disagree with the following statement: "In the design of a cache memory, the block size has an influence in the hit ratio of the cache". **JUSTIFY your answer**.

(b) (5 marks)
Briefly describe the drawbacks of both programmed I/O and interrupt-driven I/O.

(c) (10 marks)
What is the difference between instruction-level parallelism and machine parallelism? Describe the major instruction-issue policies.

Question 3:   (Total: 20 marks)

(a) (5 marks)
Write policy is among the major elements of cache design. Briefly, describe the common approaches and their impact on the performance of the cache.

(b) (5 marks)
What are the pros and cons of fixed-length and variable-length instruction encodings?

(c) (10 marks)
Draw a flowchart of the hardware implementation of unsigned binary division. Clearly explain each step.

Question 4:   (Total: 20 marks)

(a) (5 marks)
What is the difference between volatile and non-volatile memories? Give examples of both.

(b) (5 marks)
The IEEE 32-bit floating-point format uses a sign bit S, an 8-bit exponent E, and a 23-bit mantissa M. What is the equivalent decimal value for:
(1) 1 01111010 10000000000000000000000
(2) 0 10101010 11000000000000000000000

(c) (10 marks)
A given processor has 56 registers, uses 16-bit immediates, and has 221 instructions in its ISA. In a given program, 20% of the instructions take one input register and have one output register, 30% have two input registers and one output register, 25% have one input register, one output register, and take an immediate input as well, and the remaining 25% have one immediate input and one output register.
(1) For each of the four types of instructions, how many bits are required? Assume that the ISA requires that all instructions be a multiple of 8 bits in length.
(2) How much less memory does the program take up if a variable-length instruction set encoding is used as opposed to a fixed-length encoding?

Question 5:   (Total: 20 marks)

(a) (5 marks)
In a two-level memory hierarchy (cache + main memory), the average access time is 12ns. The top level of the memory system has a hit rate of 90% and an access time of 5ns. What is the access time of the lower level of the memory system?

(b) (5 marks)
Convert the following formula from reverse Polish to infix:
(1)   ABCDE+**/
(2)   ABCDE+F/+G-H/*+

(c) (5 marks)
Explain the advantages and disadvantages of:
(1)   Hardwired control unit
(2)   Micro-programmed control unit

(d) (5 marks)
Briefly explain three different applications of microprogramming.

Question 6:   (Total: 20 marks)

(a) (5 marks)
Describe the common approaches used for branch prediction during instruction pipelining.

(b) (5 marks)
Describe (briefly) how the following addressing modes work. Explain their advantages and disadvantages
(1)   Immediate addressing
(2)   Direct addressing
(3)   Register addressing
(4)   Register indirect addressing

(c) (5 marks)
What is the difference between an arithmetic shift and a logical shift?

(d) (5 marks)
What are the differences among EPROM, EEPROM, and flash memory?