National Exams December 2018

16-Mex-A3, Digital Systems & Computers

3 hours duration

NOTES:

1. If doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumptions made.

2. This is a Closed Book exam.
   Candidates may use one of two calculators, the Casio or Sharp approved models.

3. FIVE (5) questions constitute a complete exam.
   Clearly indicate your choice of any five of the six questions given otherwise the first five answers found will be considered your pick.

4. All questions are worth 12 points.
   See below for a detailed breakdown of the marking.

Marking Scheme

1. (a) 2, (b) 2, (c) 2, (d) 3, (e) 3, total = 12
2. (a) 6, (b) 3, (c) 3, total = 12
3. (a) 6, (b) 6, total = 12
4. (a) 4, (b) 4, (c) 4, total = 12
5. (a) 4, (b) 4, (c) 4, total = 12
6. (a) 4, (b) 4, (c) 4, total = 12

The number beside each part above indicates the points that part is worth

1.- (a) Using only one NAND gate build a NOT gate.

(b) Using only NAND gates build a two-input OR gate.

Draw circuits for the function g given by

$$g = \overline{\left((A+B)\cdot\bar{C} + B\bar{C}D\right)}\cdot E\cdot(A+B)$$

(c) as written above using AND, OR & NOT gates (assume 2 & 3-input gates are available).

(d) using NAND gates only (assume literal complements as well as 2 and 3-input gates are available).

(e) using NOR gates only (assume literal complements as well as 2 and 3-input gates are available).

Note: Do not use Boolean algebra or K-map to simplify function g in parts (c)-(e) above.

2.- A 3-bit counter advances through the sequence 000, 010, 100, 101, 011, 001 back to 000 and repeats.

(a) Using the standard design process for synchronous counters, show how to implement this counter using JK flip-flops. Include:

- state transition diagram,
- state transition table including flip-flop inputs, and
- a drawing of the final circuit implementing the counter.

(b) Check whether the counter is self-starting or not.

(c) Sketch the timing diagram for the counter showing its dynamic behavior for 8 clock pulses, include:

- The clock waveform CLK, containing at least six clock pulses after $t = 0$, and
- The output waveforms Q_A, Q_B & Q_C, where Q_A is the output of flip-flop A (MSB[1]), Q_B is the output of flip-flop B and Q_C is the output of flip-flop C (LSB[1]).

Assume the $\overline{CLR}$ input of all flip-flops is temporarily held LOW during the clock cycles preceding time $t = 0$, then it goes HIGH.

[1] MSB: most significant bit, LSB: least significant bit

3.- The following is a truth table of a 3-input, 4-output combinational circuit.

(a) Using K-maps obtain the simplified expressions for A, B, C and D.

(b) Implement using a PAL or PLA architecture. Justify your choice.

Inputs			Outputs			
X	Y	Z	A	B	C	D
0	0	0	0	1	1	0
0	0	1	1	0	0	0
0	1	0	0	0	1	1
0	1	1	1	1	1	1
1	0	0	1	0	1	1
1	0	1	0	1	0	1
1	1	0	0	1	1	0
1	1	1	1	1	0	1

4.- (a) Identify by marking with a X which of the following are the 4 essential components of a computer system.

__ Mouse
__ Processor (CPU)
__ Printer
__ Hard drive
__ Memory
__ Busses (address, data, control)
__ Keyboard
__ Display monitor
__ I/O ports

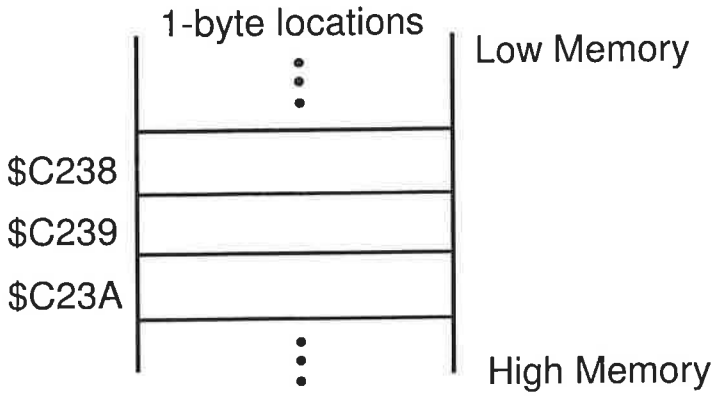
(b) Identify the main differences between a general purpose microprocessor and a microcontroller.

(c) Identify which CPU register(s) is(are) typically associated with each of the following

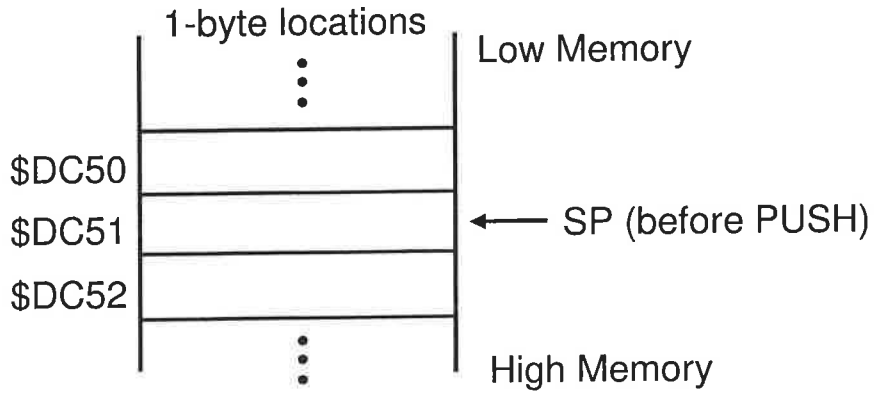
- the address of the next instruction to be executed : _____
- the next available location at the top of the stack : _____
- pointing to an array or list of data values in memory : _____
- containing the information an assembly program uses at decision making points (conditional branch statements): _____

5.- For microprocessors, such as Motorola's, that use big-endian order for storing multiple-byte variables

(a) Fill the memory block below with the result of the instruction:
"Store the 16-bit number $7A01 to address $C239"



(b) Let SP = $DC51. Fill the memory block below with the result of the instruction:
"Push the 16-bit number $7A01 onto the stack"



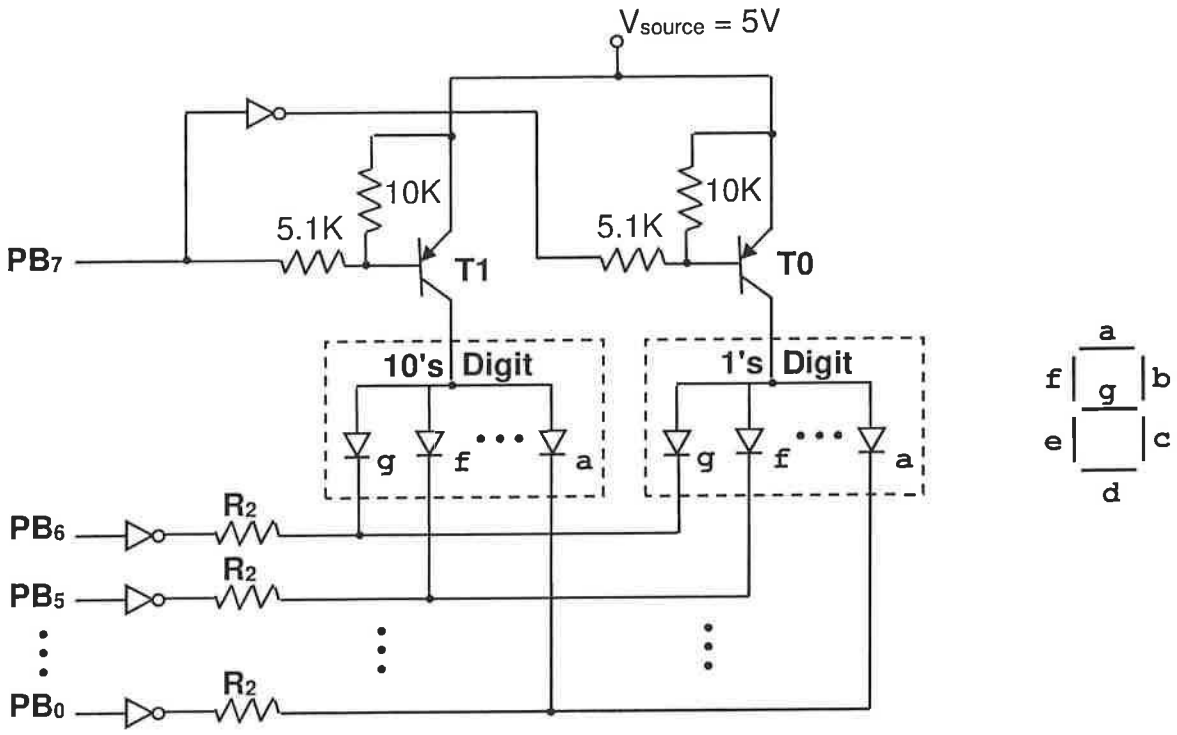
(c) What is the value of the stack pointer register SP after the PUSH?

6.- The figure below shows a circuit used to display two digits in two common-anode seven-segment LED displays. The LED arrangement for each seven-segment display is shown on the right side. Parallel Port B lines PB_7-PB_0 of a microcontroller are used to control the two-digit display. PB_7 is used for digit selection, while PB_6-PB_0 are used to determine which segments are lit. Consider that inverters are open-collector TTL inverters and transistor saturation V_{CE} value is approximately 0.3V.

(a) Provide the binary values needed in Port B lines to display the decimal number 40.

(b) From the programming point-of-view suggest the sequence of steps that will allow observing the number 40 lit on the display. Explain.

(c) Find the value for the resistors R_2 that will allow limiting the current through each LED to 10mA. When turned on, consider the nominal voltage across a LED is 2V.



Excitation Table

Q	Q+	R	S	J	K	T	D
0	0	X	0	0	X	0	0
0	1	0	1	1	X	1	1
1	0	1	0	X	1	1	0
1	1	0	X	X	0	0	1

Basic Boolean Identities

	Identity	Comments
1.	$A+0=A$	Operations with 0 and 1
2.	$A+1=1$	Operations with 0 and 1
3.	$A+A=A$	Idompotent
4.	$A+\overline{A}=1$	Complementarity
5.	$A\cdot 0=0$	Operations with 0 and 1
6.	$A\cdot 1=A$	Operations with 0 and 1
7.	$A\cdot A=A$	Idompotent
8.	$A\cdot \overline{A}=0$	Complementarity
9.	$\overline{\overline{A}}=A$	Involution
10.	$A+B=B+A$	Commutative
11.	$A\cdot B=B\cdot A$	Commutative
12.	$A+(B+C)=(A+B)+C=A+B+C$	Associative
13.	$A\cdot(B\cdot C)=(A\cdot B)\cdot C=A\cdot B\cdot C$	Associative
14.	$A\cdot(B+C)=(A\cdot B)+(A\cdot C)$	Distributive
15.	$A+(B\cdot C)=(A+B)\cdot(A+C)$	Distributive
16.	$A+(A\cdot B)=A$	Absorption
17.	$A\cdot(A+B)=A$	Absorption
18.	$(A\cdot B)+(\overline{A}\cdot C)+(B\cdot C)=(A\cdot B)+(\overline{A}\cdot C)$	Consensus
19.	$\overline{A+B+C+\ldots}=\overline{A}\cdot\overline{B}\cdot\overline{C}\cdot\ldots$	De Morgan
20.	$\overline{A\cdot B\cdot C\cdot\ldots}=\overline{A}+\overline{B}+\overline{C}+\ldots$	De Morgan
21.	$(A+\overline{B})\cdot B=A\cdot B$	Simplification
22.	$(A\cdot\overline{B})+B=A+B$	Simplification