National Exams December 2019

16-Elec-A5, Electronics

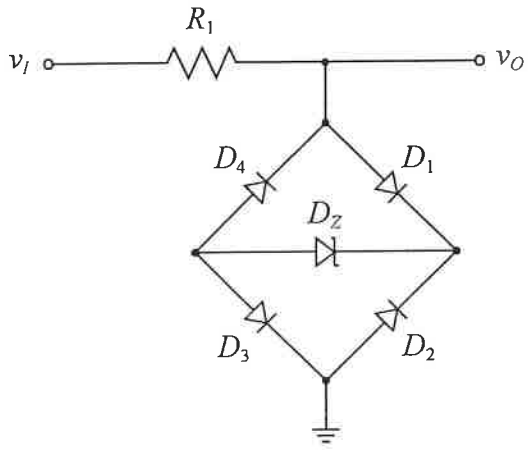
3 hours duration

Notes:

1. If any doubt exists as to the interpretation of any question, the candidate is urged to submit, within their answer, a clear statement of any assumptions made.
2. This is a **CLOSED BOOK EXAM**.
   A Casio or Sharp approved calculator is permitted.
3. Answer all **FIVE** (5) questions.
4. All questions are worth 20 marks each.
5. Please start each question on a new page and clearly identify the question number and part number, e.g. Q4(a).
6. In schematics, ground and chassis may be assumed to be common, unless specifically stated otherwise.
7. Unless otherwise specified, assume that Op-Amps are ideal and that supply voltages are ±15V.
8. If questions require an answer in essay format, clarity and organization of the answer are important. Provide block diagrams and circuit schematics whenever necessary.

QUESTION (1)

Sketch accurately the transfer characteristic (v_O versus v_I) of the following circuit for an input voltage of ±20 V. Make sure to specify all the break points and slopes. (20 points)



Given:

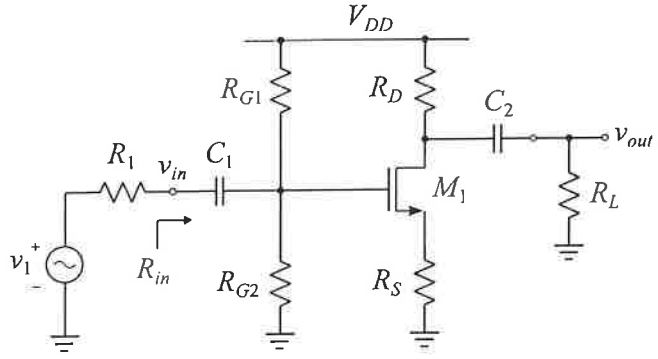
1) All diodes can be represented by a piece-wise linear model.
2) The *pn* junction diodes D_1 to D_4 have $V_{D0} = 0.65$ V and $r_D = 20\ \Omega$.
3) The zener diode D_Z, has $V_{Z0} = 8.2$ V and $r_z = 20\ \Omega$.
4) $R_1 = 1$ kΩ.

QUESTION (2)

The following is a single stage common source amplifier circuit.
Given: $V_{TH} = 1$V, $K = 4$ mA/V^2, and $\lambda = 0$

a) For a supply voltage $V_{DD} = 15$ V, design the bias circuit such that $I_D = 0.5$ mA, $V_S = 3.5$ V, and $V_D = 6$ V. Please specify the values for R_{G1}, R_{G2}, R_S and R_D. (10 points)

b) Assuming that the equivalent input resistance $R_{in} = 1.67$ MΩ, $R_1 = 100$ kΩ, $R_L = 200$ kΩ, determine the overall small signal voltage gain v_1/v_{out}. (10 points)



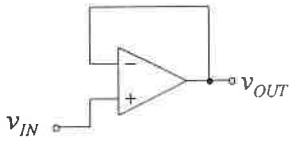
Useful formulae: for n-channel MOSFET

$$i_{DS} = K\left[(v_{GS} - V_{TH})v_{DS} - \frac{1}{2}v_{DS}^2\right] \qquad \text{triode region}$$

$$i_{DS} = \frac{1}{2}K(v_{GS} - V_{TH})^2(1 + \lambda v_{DS}) \qquad \text{saturation region}$$

QUESTION (3)

An op amp with a slew rate of 1 V/μs and a unity-gain bandwidth, f_t of 1 MHz is connected in the unity-gain follower configuration.



a) What is the largest possible input voltage step for which the output voltage waveform can still produce exponentially rising and falling waveforms? (8 points)

b) For this input voltage, find the 10% to 90% rise time. (6 points)

c) If the input step is 10 times larger than the voltage that you have found in part (a), find the new 10% to 90% rise time. (6 points)

Given:

Supply Voltage = ±10 V

Useful Formulae:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1+s/\omega_t}, \quad v_{OUT}(t) = V\left(1-e^{-\omega_t t}\right)$$

QUESTION (4)

In the following CMOS inverter, the threshold voltages of the *n*- and *p*-channel transistors are V_{Tn} and $-|V_{Tp}|$, respectively:

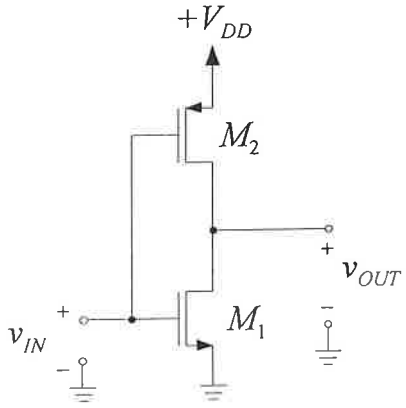
a) Draw the input to output voltage transfer characteristic (VTC) for this inverter. Express and label clearly all voltage levels on the VTC plot. (20 points)

b) Indicate the noise margins NM_L and NM_H on the VTC.

c) Indicate the logic high and low output voltage levels V_{OH}, V_{OL} on the VTC.

d) Indicate the logic high and low input voltage levels V_{IH}, V_{IL} on the VTC.

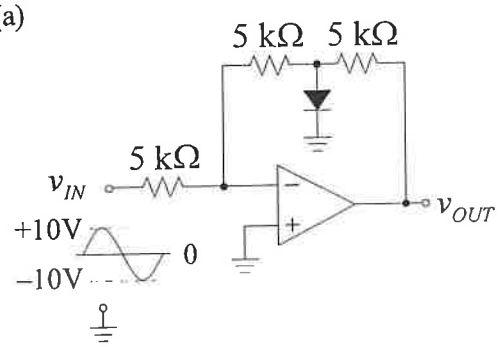
e) Indicate clearly the mode of operation in each region of the VTC.



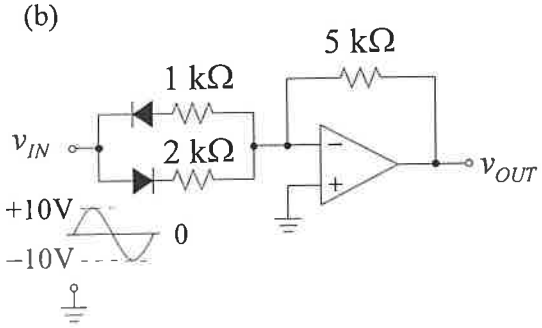
QUESTION (5)

In the following circuits, assume that the diode is ideal and has a forward voltage drop of 0.7V, and all op amps are ideal and with supply voltages of ±15 V. Sketch the output waveform for one complete sine wave input cycle. (20 points)

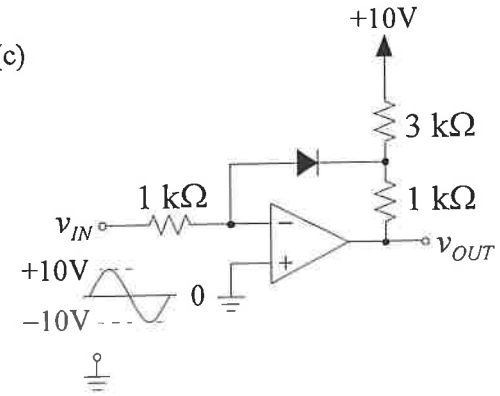
(a)



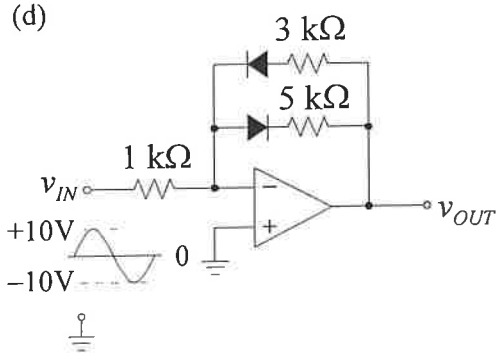
(b)



(c)



(d)



(e)