National Exams May 2016

98-Comp-A1, Electronics

3 hours duration

NOTES:

1. If doubt exists as to the interpretation of any question, the candidate is urged to indicate, with the answer, a clear statement of any assumptions made.

2. This is a OPEN BOOK exam.
   Any non-communicating calculator is permitted.

3. FIVE (5) questions constitute a complete exam paper.
   The first 5 questions as they appear in the answer book will be marked.

4. Each question is of equal value.

Question 1 (20 marks)

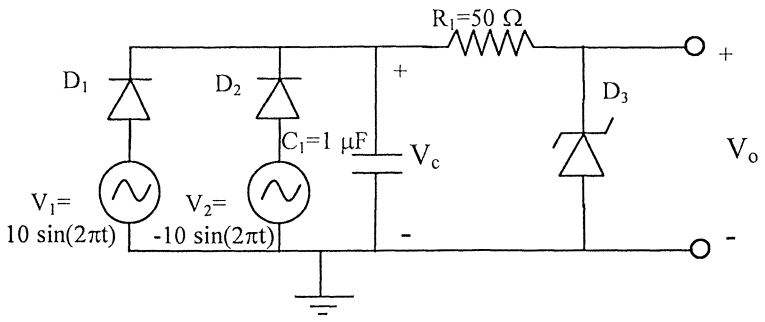

Figure 1. Diodes D_1, D_2 have a forward voltage drop V_D=0.7V. Diode D_3 has a maximum reverse voltage of 5.1V.

For the circuit shown in Figure 1 is in steady state:

a) Sketch V_1, V_2 and V_o as a function of time, indicating peak voltages.

b) Sketch V_c, as a function of time, indicating peak voltages.

c) What is the peak current through R_1?

d) What power rating would you choose for D_3?

Question 2 (20 marks)

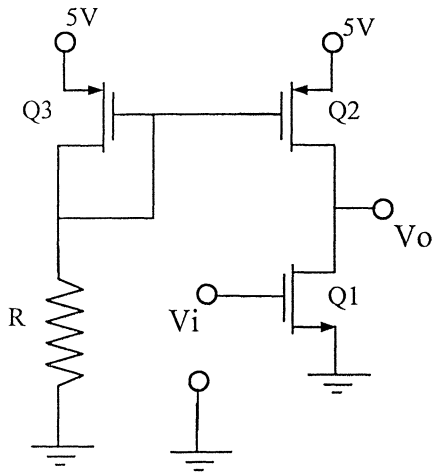

Figure 2. $k_n' = \mu_n C_{ox} = 1$ mA/V^2, W/L=10, $|V_t| = 1$V, $V_A = 100$V assume $\lambda = 0$.

For the circuit shown in Figure 2:

a) Find a value for R that will result in $I_{D,Q3} = 0.5$mA?

b) Draw a small signal equivalent model for the circuit.

c) What is the small signal AC gain of the circuit?

Question 3 (20 marks)

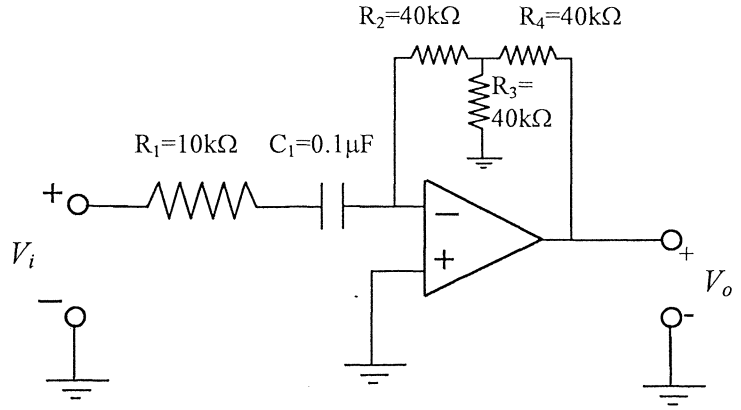

Figure 3.

For the circuit shown in Figure 3:

a) Derive the transfer function $\frac{V_o(j\omega)}{V_i(j\omega)}$ for the circuit shown in Figure 3, assuming the op-amp is ideal.

b) Sketch the frequency response, indicating 3dB frequencies for this circuit.

c) If $V_i(t)$=10sin(120πt) V, find $V_o(t)$.

Question 4(20 marks)

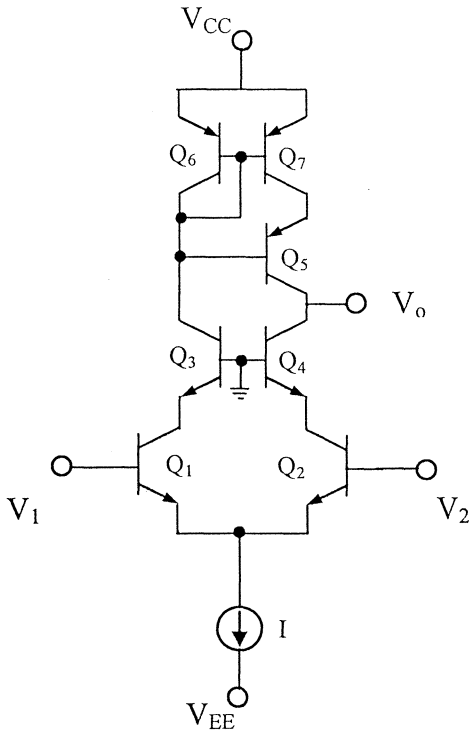

Figure 4. I=0.2mA, β=100, V_A=100V.

For the circuit shown in Figure 4:

a) Find the input resistance Ri.

b) Find the output resistance Ro.

c) Find the amplifier transconductance G_m.

d) Find the open-circuit voltage gain for the amplifier.

Question 5 (20 marks)

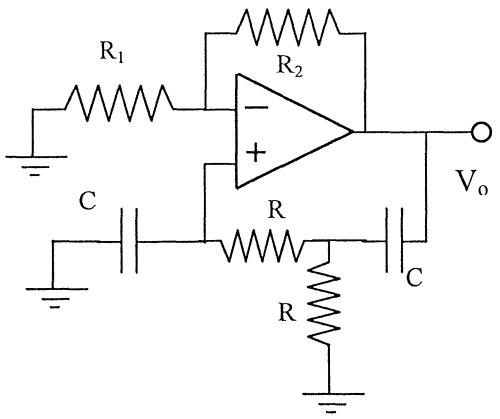

Figure 5. R=10kΩ, C=0.1μF

For the circuit shown in Figure 5:

a) Find the loop gain expression.

b) Find the condition for zero loop-phase.

c) Choose component values R_1 and R_2 to sustain oscillation.

Question 6 (20 marks)

a) Synthesize a CMOS logic circuit to implement $Y= \overline{AB(C+D)}$.

b) Size transistors in your circuit. The minimum length is 1 μm and the basic inverter uses n=2 and p=5.

c) Synthesize the function in a) using pass transistor logic.

Question 7 (20 marks)

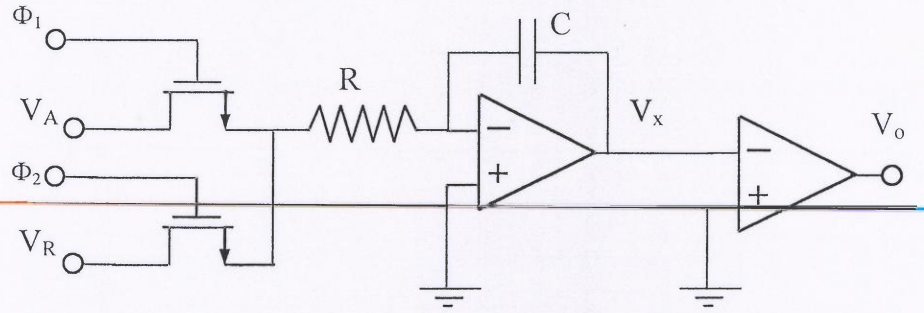

Figure 6. $V_A<0$, V_R is a positive reference. The capacitor is initially discharged. At t=0 Φ_1 goes high, Φ_2 goes low. For $t>T_1$ Φ_1 goes low, Φ_2 goes high. At $t=T_2$ the comparator output switches.

a) Sketch $V_x(t)$.

b) Find the slope of $V_x(t)$.

c) Find an expression for T_2/T_1.

d) What are the limitations of the application of this circuit?

Marking Scheme

1. 20 marks total (4 parts, 5 marks each)
2. 20 marks total (a. 10 marks, b. 5 marks, c. 5 marks)
3. 20 marks total (a. 10 marks, b. 5 marks, c. 5 marks)
4. 20 marks total (4 parts, 5 marks each)
5. 20 marks total (a. 10 marks, b. 5 marks, c. 5 marks)
6. 20 marks total (a. 5 marks, b. 5 marks, c. 10 marks)
7. 20 marks total (4 parts, 5 marks each)

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