National Exams May 2017

16-Elec-B6, Integrated Circuit Engineering

3 hours duration

NOTES:

1. This is a closed-book examination. No material is permitted to be brought to the examination.
2. There are six (6) questions in the examination paper. Any five (5) questions constitute a complete paper. Only the first five questions as they appear in the answer sheets of candidates will be graded.
3. The marks for each question are indicated in the examination paper. The total marks of the examination are 100.
4. Scientific calculators without wireless communication capability are allowed.
5. Formulae and constants are provided at the end of the examination paper.
6. If a doubt exists as to the interpretation of any question of the examination, candidates are urged to submit with their answer sheets, a clear statement of any assumption made.

Q1. Consider a step voltage v_s=1 V (i.e. v_s=0 if t<0 and v_s=1V if t≥0) applied to node 1 of a lossless transmission line that is terminated with a static CMOS inverter, as shown in Fig.Q1. Let the characteristic impedance of the transmission line be Z_o. Further, let the propagation delay of the signal traveling from one end of the transmission line to the other end be τ. Assume the input impedance looking into node 1 of the transmission line is Z_o. Further, assume the input impedance of the static CMOS inverter is infinity, i.e. Z_L=∞.

Fig.Q1.

1) Sketch the waveform of the voltages at nodes 1 and 2 for time duration 0-5τ if the source impedance is Z_s=Z_o (6 marks).

2) Sketch the waveform of the voltages at nodes 1 and 2 for time duration 0-5τ if the source impedance is Z_s=5Z_o (7 marks).

3) Sketch the waveform of the voltages at nodes 1 and 2 for time duration 0-5τ if the source impedance is Z_s=Z_o/5 (7 marks).

The detailed steps of your solutions must be provided to support your answers.

Q2. Design an one-bit full adder using combinational static logic circuits with A and B the inputs, C_{in} the carry-in, S_o the sum, and C_o the carry-out of the adder. Assume that the load capacitance of S_o and that of C_o of the adder are the same as that of a generic static CMOS inverter whose aspect ratios are $(W/L)_n$ for nMOS transistor and $(W/L)_p$ for pMOS transistor.

1) Show the combinational static logic circuit of C_o and that of S_o (10 marks).

2) Find the aspect ratio of all the transistors of the full adder with the constraint that the High-to-Low and Low-to-High propagation delays of S_o are the same as those of the inverter. The same constraint holds for C_o (10 marks).

Q3. Design a one-bit full adder using NP-Domino logic circuits with A and B the inputs, C_{in} the carry-in, S_o the sum, and C_o the carry-out of the adder. Assume that the load capacitance of S_o and that of C_o of the adder are the same as that of a generic static CMOS inverter whose aspect ratios are $(W/L)_n$ for nMOS transistor and $(W/L)_p$ for pMOS transistor.

a. Show the NP-Domino logic circuit of C_o and that of S_o (10 marks).

b. Find the aspect ratio of all the transistors of the full adder with the constraint that the High-to-Low and Low-to-High propagation delays of S_o are the same as those of the inverter. The same constraint holds for C_o (10 marks).

Q4. This question consists of three (3) sub-questions. All sub-questions must be answered.

1) A complementary static CMOS logic circuit is shown in Fig.Q4.1. Assume the bulk of all nMOS transistors are connected to the ground and that of all pMOS transistors are connected to V_{DD}.

   a. Determine which transistor is subject to body effect and the effect of body effect (4 marks).

   b. Assume that input B leads input A. As a designer, how would you modify the design to minimize the effect of body effect (2 marks).

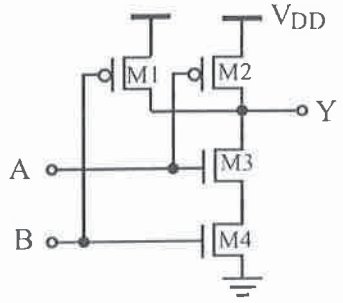

Fig.Q4.1.

2) A dynamic CMOS logic circuit is shown in Fig.Q4.2.

   a. Determine the output of the circuit in pre-charge and evaluation phases (4 marks).

b. In the evaluation phase, for some specific inputs, the output voltage drops below V_{DD} (neglect the voltage drop across the pMOS transistor) due to charge sharing. Identify these inputs and give your reasons (3 marks).

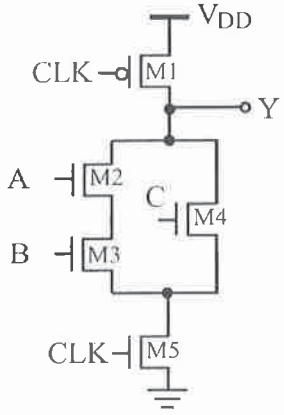

Fig.Q4.2.

3) The C²MOS dynamic logic circuit shown in Fig.Q4.3 implements a D-flipflop.

a. Determine the logic expression at nodes A and B when CLK=0 and CLK=1, respectively (3 marks).

b. Clock skew is critical to dynamic logic circuits. Show that this circuit is not sensitive to clock skew (4 marks).

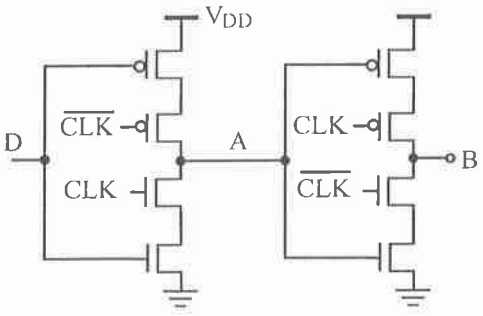

Fig.Q4.3.

Q5. This question consists of three (3) sub-questions. All sub-questions must be answered.

1) A complementary pass transistor (CPL) implementation of an AND2 gate is shown in Fig.Q5.1. Assume $V_{TN}=|V_{TP}|=V_T$, where V_{TN} and V_{TP} are the threshold voltages of nMOS and pMOS transistors, respectively.

a. Determine V_{o1} when $A=B=V_{DD}$. Neglect the leakage of reverse biased pn-junctions (3 marks).

b. Determine whether the inverter consumes static power or not, and give your reason (4 marks).

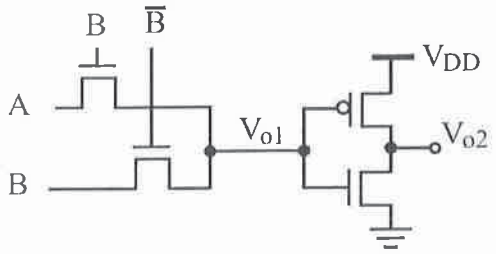

Fig.Q5.1.

2) True-single-clock-phase (TSPC) logic circuits are widely used due to their simple configuration subsequently small propagation delay and low power consumption. Fig.Q5.2 shows the schematic of a positive edge triggered D flipflop realized using TSPC logic. Show that it is indeed a positive edge triggered D flipflop (7 marks).

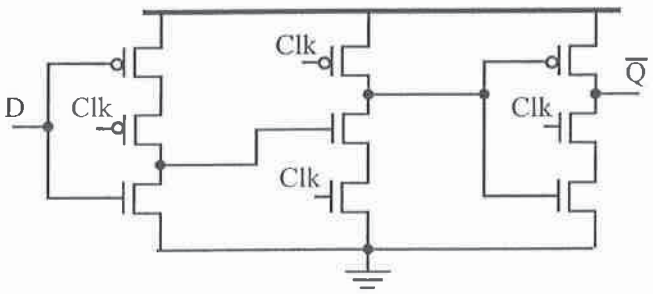

Fig.Q5.2.

3) The schematic of a static CMOS inverter output buffer is shown in Fig.Q5.3. The waveform of v_{in} and that of v_{out} are shown in the figure. Sketch the waveform of the capacitor current i_{CL}, on-chip supply voltage $V_{dd,on\text{-}chip}$, and on-chip ground $V_{ss,on\text{-}chip}$ (7 marks)

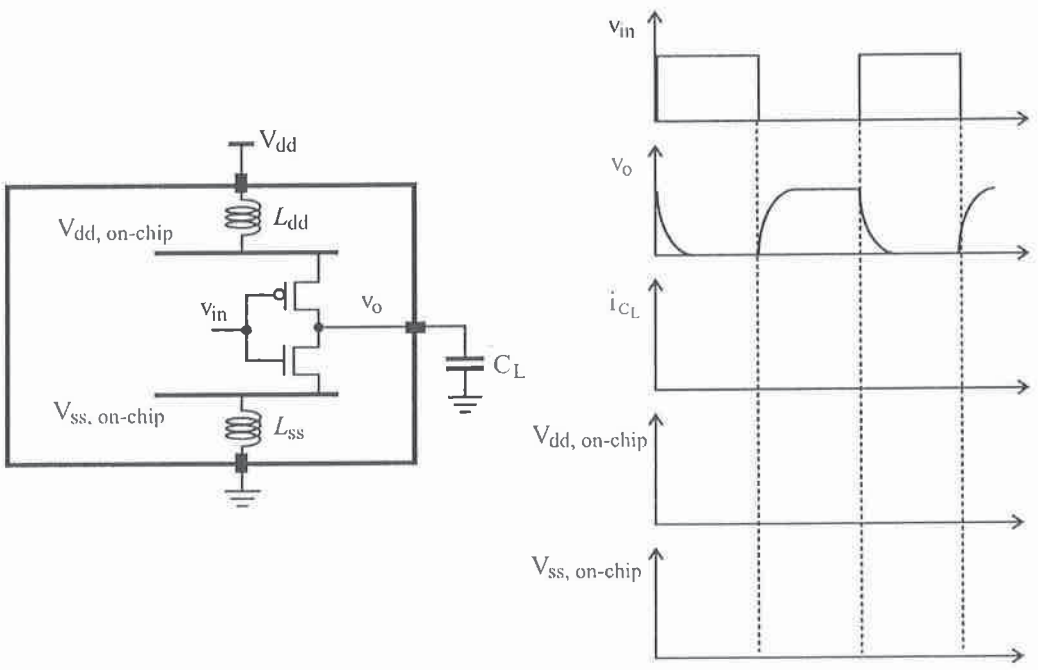

Fig.Q5.3.

Q6. The layout of a static CMOS inverter is shown in Fig.Q6 with process parameters given in "Formulae and Constants" section at the end of the examination paper. Neglect sidewall capacitances, overlap capacitances, and fringe capacitances. A 1 GHz square wave is applied to the input of the inverter. Assume the voltage swing of the input and that of the output are 0~1.2 V. Determine the dynamic power dissipation of the inverter (20 marks).

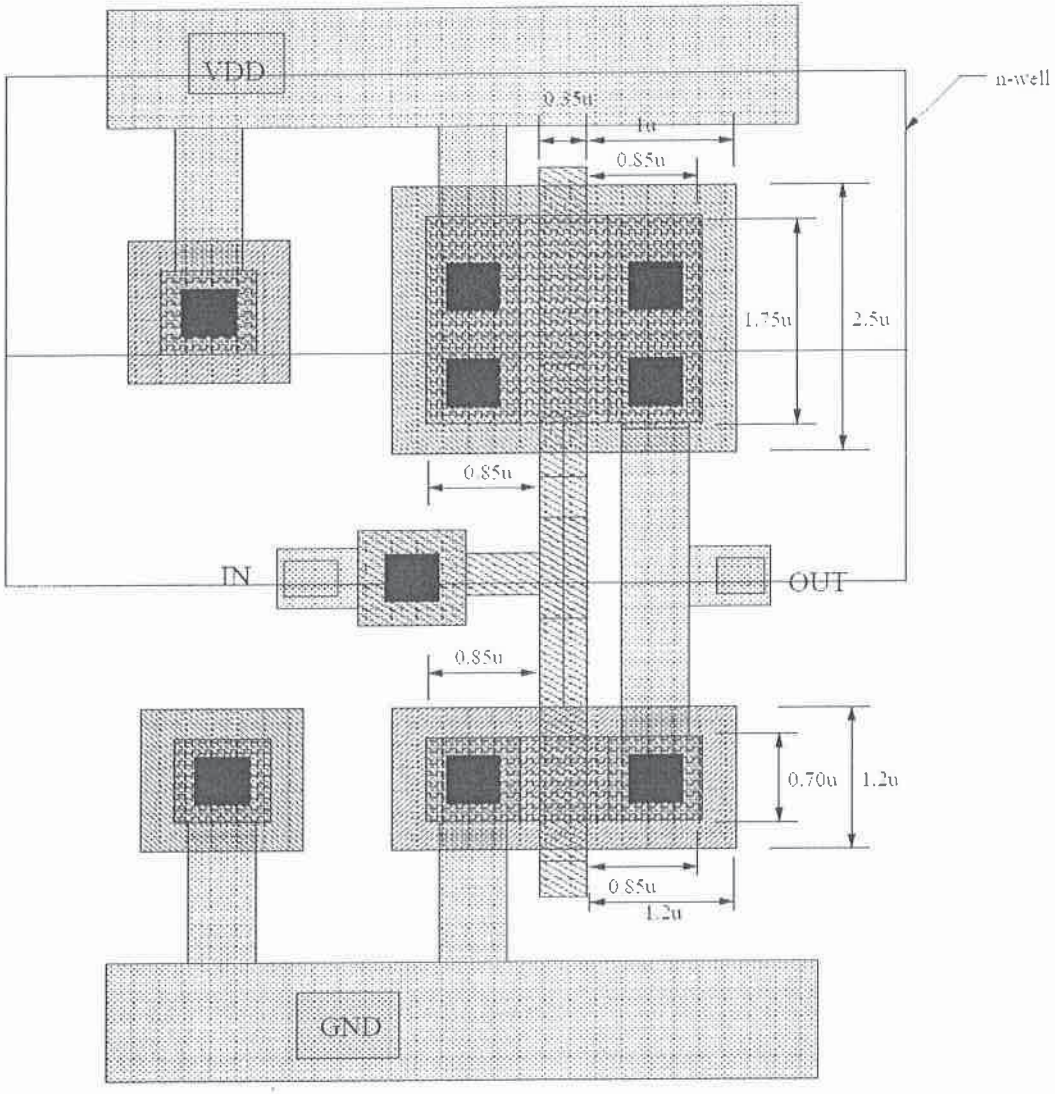

Fig.Q6 (Legend: u: μm).

Formulae and Constants

1. Large-signal pn-junction capacitance per unit area

$$C_J = \frac{2\sqrt{\phi_o}}{V_{R1} - V_{R2}}\left(\sqrt{V_{R2} + \phi_o} - \sqrt{V_{R1} + \phi_o}\right) C_{Jo},$$

where

$$C_{Jo} = \sqrt{\frac{q\varepsilon_s}{2}\frac{N_A N_B}{N_A + N_B}\frac{1}{\phi_o}},$$

$$\phi_o = \phi_t \ln\left(\frac{N_A N_D}{n_i^2}\right),$$

V_{R1} and V_{R2} are the two reverse biasing voltages of the pn-junction.

2. Voltage reflection coefficient

$$\Gamma_V = \frac{Z_L - Z_o}{Z_L + Z_o},$$

where Z_L and Z_o are the load and characteristic impedances of the transmission line, respectively.

3. Constants

Constant	Value	Description
q	1.6×10^{-19}C	Charge of an electron.
ε_s	1.05×10^{-12} F/cm	Permittivity of silicon.
n_i	1.5×10^{10}cm^3	Intrinsic charge carrier concentration of silicon at 300K.
ϕ_t	26 mV	Thermal voltage at 300K.
C_{ox}	3.5 fF /um^2	Gate capacitance per unit area
$N_{A,sub}$	10^{16}/cm^3	Doping of p-substrate
$N_{D,nwell}$	10^{16}/cm^3	Doping of n-well
N_D	10^{19}/cm^3	Doping of the source and drain of nMOS transistors
N_A	10^{19}/cm^3	Doping of the source and drain of pMOS transistors