National Exams December 2019

**16-Elec-A4, Digital Systems & Computers**

3 hours duration

## NOTES:

1. If doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumptions made.

2. This is a Closed Book exam.
   Candidates may use one of two calculators, the Casio or Sharp approved models.

3. FIVE (5) questions constitute a complete exam.
   Clearly indicate your choice of any five of the six questions given otherwise the first five answers found will be considered your pick.

4. All questions are worth 12 points.
   See below for a detailed breakdown of the marking.

### Marking Scheme

1. (a) 3, (b) 3, (c) 3, (d) 3, total = 12
2. (a) 4, (b) 4, (c) 4, total = 12
3. (a) 3, (b) 6, (c) 3, total = 12
4. (a) 3, (b) 3, (c) 3, (d) 3, total = 12
5. (a) 6, (b) 6, total = 12
6. (a) 4, (b) 8, total = 12

The number beside each part above indicates the points that part is worth

**1.-** Given the following function:

$$f = \bar{A} \cdot C \cdot D + A \cdot \bar{B} \cdot C + A \cdot B \cdot D + \bar{A} \cdot \bar{C} \cdot D + \bar{A} \cdot \bar{B} \cdot C \cdot \bar{D}$$

(a) Prepare its truth table.

(b) Express $f$ in canonical sum-of-products (SoP) form using the shorthand $\sum m_i$ notation, where $m_i$ are the function minterms.

(c) Express $f$ in minimized SoP form.

(d) Check if the minimized expression found in (c) is hazard-free. Justify.

If it is not hazard-free provide the smallest SoP hazard-free expression for $f$.

**2.-** (a) Implement the following Boolean functions by using 8:1 multiplexers:

i) $f_1(A,B,C) = \sum m_i(1,4,6)$, We are also told that the input combinations ABC = 011 and ABC = 111 are not of concern for $f_1$.

ii) $f_2(A,B,C) = \prod M_i(0,1,2,5)$.

(b) Implement the same Boolean functions $f_1$ & $f_2$, given above in part (a), using one 4:1 multiplexer for each function.

(c) Implement all 3 Boolean functions below by using one 3:8 decoder and three OR gates. Specify all the decoder inputs.

i) $f_1(A,B,C) = A \cdot (\bar{B} + C)$

ii) $f_2(A,B,C) = \sum m_i(0,3,4)$

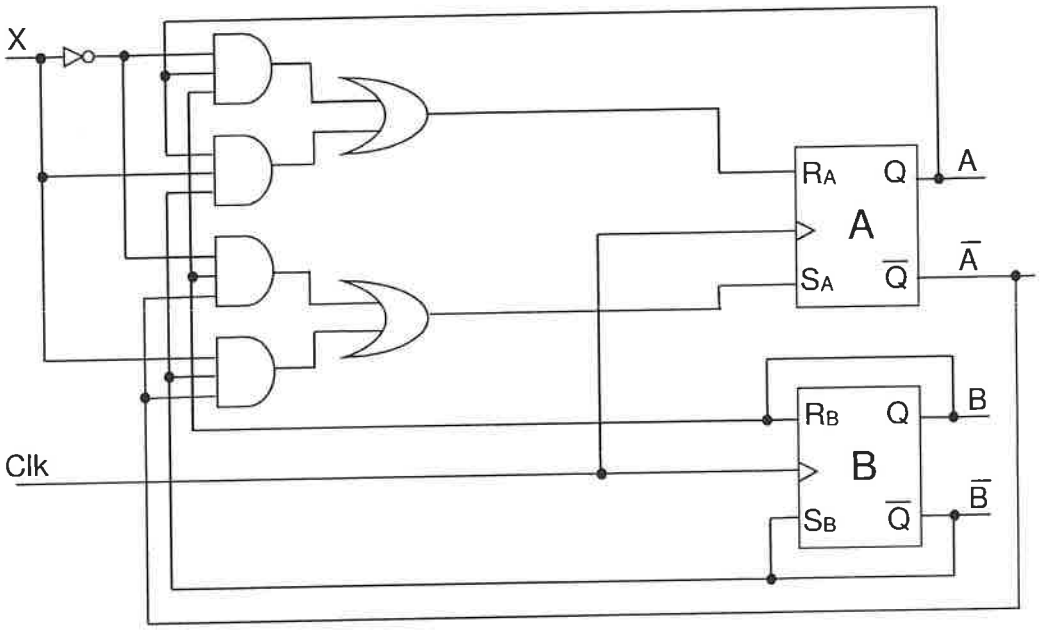
iii) $f_3(A,B,C) = A \cdot B \cdot C + B \cdot \bar{C}$

**3.-** The following circuit contains two RS flip-flops.

(a) Write the logic expressions for $R_A$, $S_A$, $R_B$ and $S_B$.

(b) Obtain the state transition table for the circuit.

(c) Sketch the state transition diagram for the circuit.



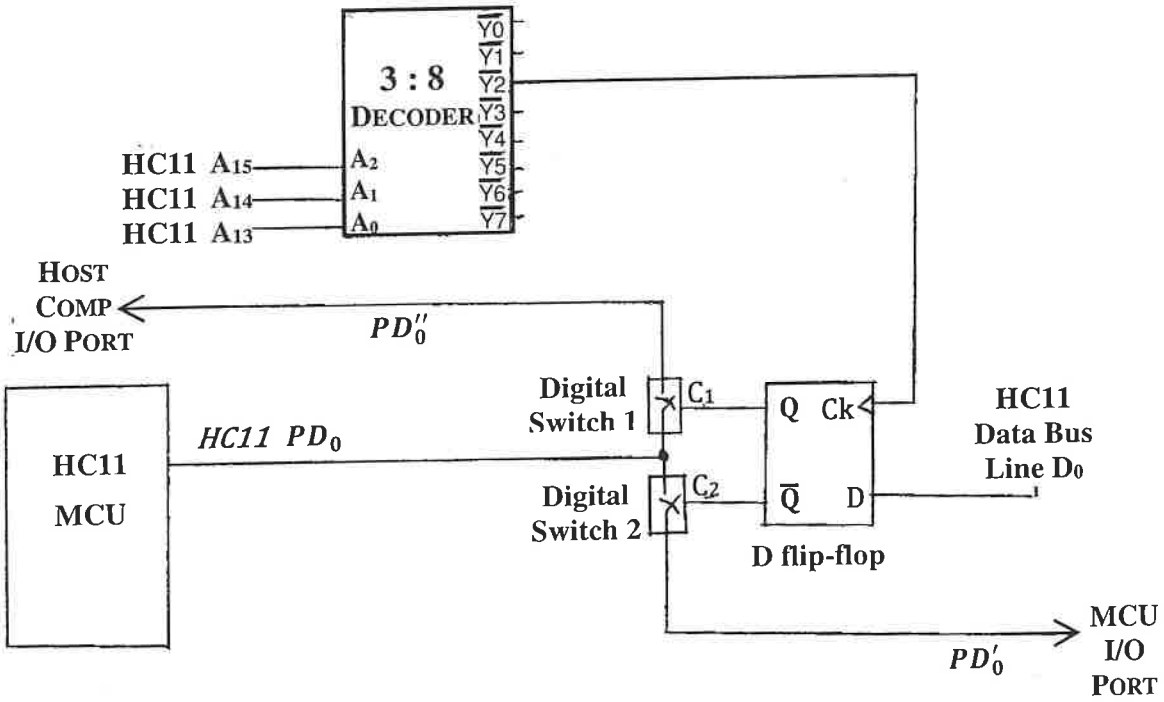
4.- The diagram below shows the use a D flip-flop governing two digital switches in order to route line $PD_0$ of the HC11 microcontroller unit (MCU) to one of two connectors: the HOST computer I/O port or the MCU I/O port connector.
Digitals switches close when control input C is at a logic '1' and remain open when C is '0'.
HC11 address lines $A_{15}$ - $A_{13}$ are connected to the 3 address inputs of a 3:8 decoder as shown in the figure, the most significant address input of the decoder is $A_2$ and the least significant is $A_0$. Assume the decoder is enabled and towards the end of the execution of each instruction cycle all its active-low outputs $\bar{Y}_0$ - $\bar{Y}_7$ go back to their inactive logic '1' state.
The least significant data bus line of the HC11 ($D_0$) is connected to the flip-flop D input.
Knowing that instruction
**ldaa #$xx** means load HC11 CPU register accumulator A with hexadecimal value **xx**, and
**staa $zzzz** means store the value in accumulator A to address $**zzzz,**
which of the following set of instructions will direct HC11 line $PD_0$ to the HOST computer I/O port, which to the MCU I/O port connector and which will not affect the current routing. Mark your choice with an **X** and justify your selection in each case.

(a) ldaa #$10, staa $8000 [ ] HOST Comp I/O port, [ ] MCU I/O port, [ ] No Action

(b) ldaa #$29, staa $4000 [ ] HOST Comp I/O port, [ ] MCU I/O port, [ ] No Action

(c) ldaa #$B4, staa $5000 [ ] HOST Comp I/O port, [ ] MCU I/O port, [ ] No Action

(d) ldaa #$05, staa $2500 [ ] HOST Comp I/O port, [ ] MCU I/O port, [ ] No Action



5.- (a) Describe the algorithm of a short assembly program, including any additional routines needed, in charge of [6 pts]

1. Reading ONE (1) character (char) received through an asynchronous serial port,
2. Converting that char received to lowercase if uppercase, or viceversa (assume the char received is a letter), and
3. Transmitting the char obtained in Step 2 above through the asynchronous serial port using interrupts.

You can use a subroutine called `inchar` starting at address $FFCD_{hex}$. This subroutine loops until a character is received by the input serial port then returns the ASCII character in a CPU register called accumulator A (ACCA).

Assume the asynchronous serial port has been initialized already including a serial line speed of 9600 baud.

Assume standard serial port registers: status (SR), control (CR), transmit data (TDR) and receive data (RDR) are memory mapped and their addresses available.

(b) Both input and output serial channels support RS-232 levels, this is, the microprocessor board receive data (RxD) line is coupled to the channel through RS-232 receivers and the transmit data (TxD) line is coupled to the channel through RS-232 drivers.

Assume the character 'U' is received by your program through the serial port.

Once your program runs sketch the time waveforms for:

(i) the serial bit stream on the TxD line in the board before the RS-232 drivers, and

(ii) the same serial bit stream in (i) above on the transmit line of the RS-232 cable connected to the board serial port connector.

Label each bit appropriately according to their position and role in the frame.

Include time scale values and voltage scale values for each case. [6 pts]

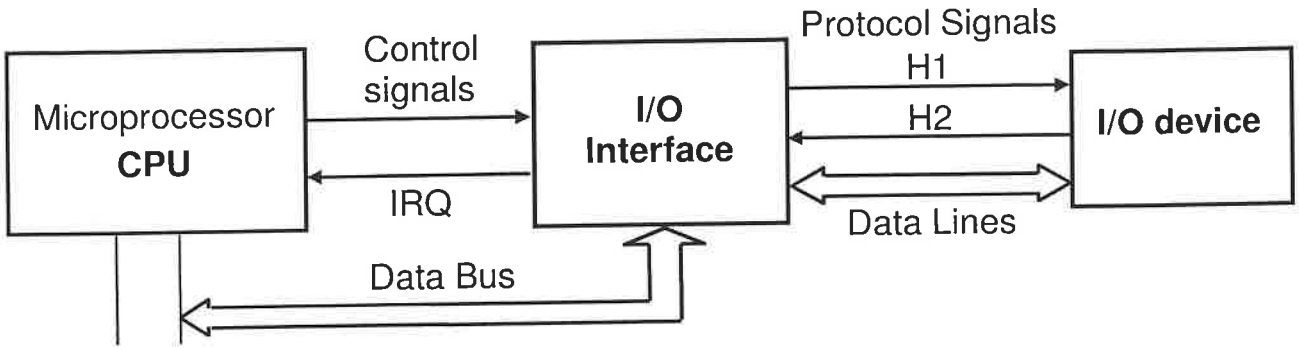
Assume CMOS logic levels are used within the microprocessor board.

ASCII value for 'U' is $55_{hex}$

ASCII value for 'u' is $75_{hex}$

hex stands for hexadecimal

**6.-** The diagram below shows the main elements participating in the parallel I/O of data.




(a) Mention the two methods used in programming the CPU to communicate with the I/O interface in order to become aware of new available data, or interface readiness, and transfer the data between the two in the corresponding direction.

Which of the two methods is more efficient? Explain.

(b) i. Mention two parallel I/O protocols used for implementing the data exchange between the I/O interface and the external I/O device.

ii. Describe the main steps involved in these protocols for the INPUT of data from the I/O device and for the OUTPUT of data to the I/O device, separately.
Mention which protocol signal H1 or H2 work for signaling VALID DATA in data lines or ACKNOWLEDGEMENT of data reception in each case.

## Excitation Table

| Q | Q+ | R | S | J | K | T | D |
|---|---|---|---|---|---|---|---|
| 0 | 0 | X | 0 | 0 | X | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | X | 1 | 1 |
| 1 | 0 | 1 | 0 | X | 1 | 1 | 0 |
| 1 | 1 | 0 | X | X | 0 | 0 | 1 |

## Basic Boolean Identities

| | Identity | Comments |
|---|---|---|
| 1. | $A+0=A$ | Operations with 0 and 1 |
| 2. | $A+1=1$ | Operations with 0 and 1 |
| 3. | $A+A=A$ | Idompotent |
| 4. | $A+\overline{A}=1$ | Complementarity |
| 5. | $A\cdot 0=0$ | Operations with 0 and 1 |
| 6. | $A\cdot 1=A$ | Operations with 0 and 1 |
| 7. | $A\cdot A=A$ | Idompotent |
| 8. | $A\cdot \overline{A}=0$ | Complementarity |
| 9. | $\overline{\overline{A}}=A$ | Involution |
| 10. | $A+B=B+A$ | Commutative |
| 11. | $A\cdot B=B\cdot A$ | Commutative |
| 12. | $A+(B+C)=(A+B)+C=A+B+C$ | Associative |
| 13. | $A\cdot(B\cdot C)=(A\cdot B)\cdot C=A\cdot B\cdot C$ | Associative |
| 14. | $A\cdot(B+C)=(A\cdot B)+(A\cdot C)$ | Distributive |
| 15. | $A+(B\cdot C)=(A+B)\cdot(A+C)$ | Distributive |
| 16. | $A+(A\cdot B)=A$ | Absorption |
| 17. | $A\cdot(A+B)=A$ | Absorption |
| 18. | $(A\cdot B)+(\overline{A}\cdot C)+(B\cdot C)=(A\cdot B)+(\overline{A}\cdot C)$ | Consensus |
| 19. | $\overline{A+B+C+\ldots}=\overline{A}\cdot\overline{B}\cdot\overline{C}\cdot\ldots$ | De Morgan |
| 20. | $\overline{A\cdot B\cdot C\cdot\ldots}=\overline{A}+\overline{B}+\overline{C}+\ldots$ | De Morgan |
| 21. | $(A+\overline{B})\cdot B=A\cdot B$ | Simplification |
| 22. | $(A\cdot\overline{B})+B=A+B$ | Simplification |