National Exams December 2018

17-Phys-A5-B Analog and Digital Electronic Circuits

3 hours duration

NOTES:

1. If doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumptions made.

2. This is an OPEN BOOK EXAM.
   Any non-communicating calculator is permitted.

3. Answer all SIX (6) questions.

4. Please start each question on a new page and clearly identify the question number and part number, e.g. Q1(a).

5. If questions require an answer in essay format, clarity and organization of the answer are important. Provide block diagrams and circuit schematics whenever necessary.

Marking Scheme

1. (a) 15 marks
2. (a) 10 marks; (b) 10 marks;
3. (a) 5 marks; (b) 5 marks (c) 5 marks; (d) 5 marks
4. (a) 10 marks; (b)5 marks
5. (a) 10 marks; (b) 5 marks
6. (a) 5 marks; (b) 10 marks

Question1

In the circuit shown in Fig.1 assume V_{BE}= 0.7V, β=100 and neglect Early effect ($V_A = \infty$) for all transistors.
(a) Calculate the small-signal midband gain $A_M = v_o/v_i$.

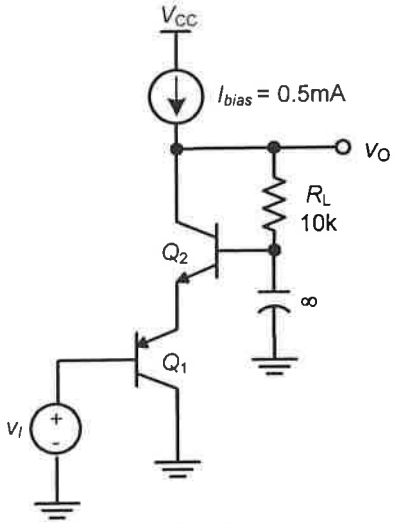

Fig. 1

Question2

Consider the circuit shown in Fig.2. R_1=R_2=R_3=1kΩ, R_4=10kΩ, C_1=1μF.
(a) Derive an expression for the voltage gain, v_o/v_i. Assume ideal Op-Amps.
(b) Sketch the Bode plot (dB vs frequency in rad/sec) for the magnitude of the transfer function, v_o/v_i.

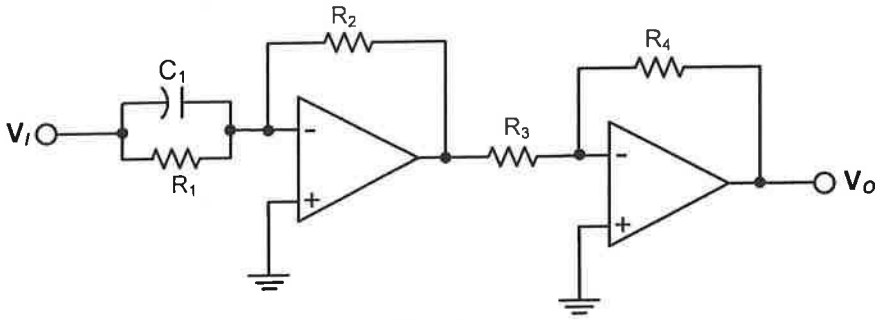

Fig. 2

Question3:

Figure 3 shows a MOS amplifier. Consider I_{bias} = 2mA, the source resistor R_{sig}=10KΩ, the load C_L = 50fF, Assume all the transistors are in active region and they have same aspect ratios $(\frac{W}{L})$ =10, $\mu_n C_{ox}$=$\mu_p C_{ox}$= 100μA/V², V_{An} = $|V_{Ap}|$ = 20V, C_{gs}=50fF and C_{gd}= 20fF for all the transistors.

(a) Identify the kind of this MOS amplifier.
(b) Find the currents I_{D1} (neglect Early effect only here in (b))
(c) Calculate the low frequency dc gain $A_v = v_o/v_{sig}$.
(d) Calculate the 3-dB frequency, f_H, of this amplifier using open circuit time constants technique.

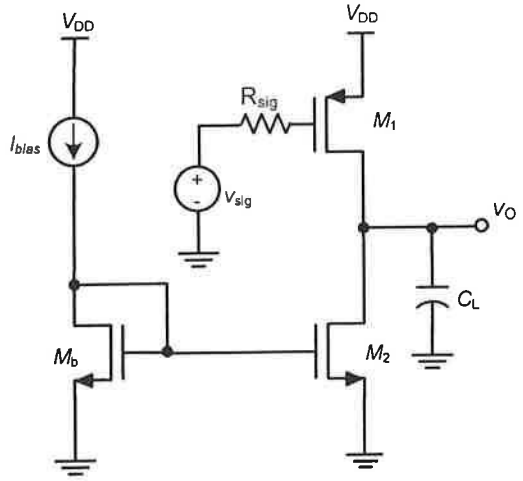

Fig. 3

Question 4

For the amplifier, shown in Fig. 4, it is desired to obtain a precise gain v_O/v_S using feedback. Assume that $g_{m1} = g_{m2} \neq g_{m3}$, $\beta_3 \neq \infty$ (Betta of Q_3), and $r_{o1} = r_{o2} = r_{o3} = \infty$. I_{bias} is an ideal current source. Assume transistors are in active regions.

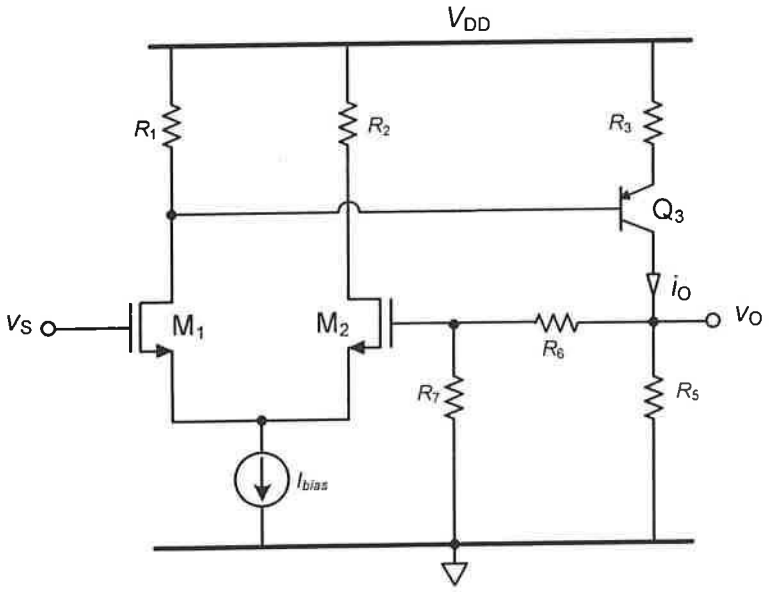

Fig. 4

(a) Use the methods of feedback analysis to find the expression of the gain v_O/v_S.
(b) Explain why the base of Q_3 is connected to the drain of M_1 and not to the drain of M_2.

Question 5

An 8-bit digital-to-analog converter (DAC) shown in Fig 5 has a voltage reference V_{ref} = 5 V.

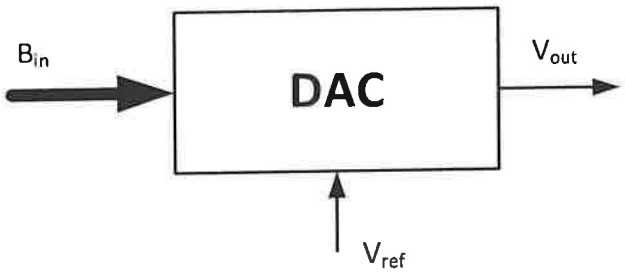

Fig. 5

(a) What is the output voltage V_{out} when the binary input Bin = 10110100.
(b) Find the least significant bit voltage V_{LSB}.

Question 6

The circuit in Fig.6 shows the pull-down network (PDN) for a static CMOS logic gate that implements the function Y.

(a) Find the pull-up network (PUN) that corresponds to the PDN and hence complete the CMOS logic circuits.
(b) What is the Boolean function realized.

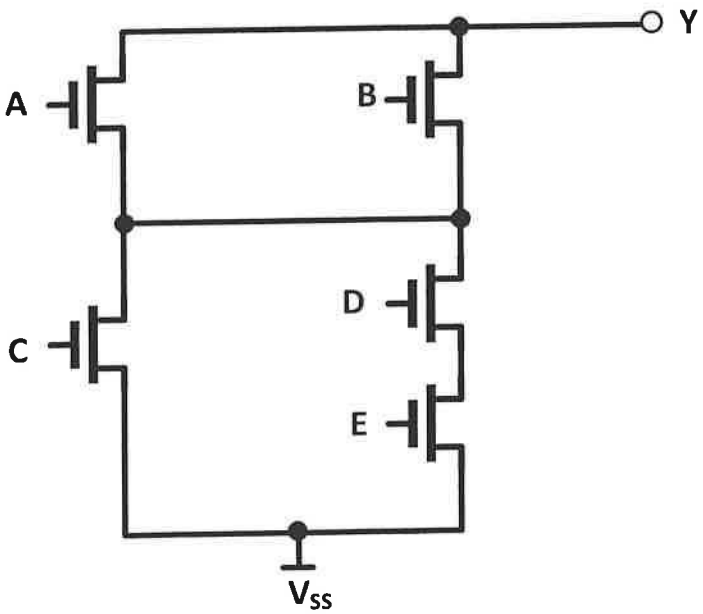

Fig.6