National Exams December 2018

16-Mex-A2, Circuits and Electronics

3 hours duration

NOTES:

1. If doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumptions made.

2. This is a CLOSED BOOK EXAM. An approved Casio or Sharp model calculator is permitted.

3. This exam **has two parts Part A Circuits and Part B Electronics**. Answer either 3 questions from Part A and two questions from Part B or 2 questions from Part A and 3 questions from Part B a total of 5 questions answered. Indicate in the front page of your answer book which questions you want to be marked.

4. Please indicate which part the question you are answering is from ether Part A or Part B. Start each new question on a new page and number and part number e.g. Q4(a).

5. For the Part B Electronics part of the exam in schematics, ground and chassis may be assumed to be common, unless specifically stated otherwise. Also, unless otherwise specified, assume that Op-Amps are ideal and that supply voltages are

6. If questions require an answer in essay format, clarity and organization of the answer are important. Provide block diagrams and circuit schematics whenever necessary.

7. For the Part A Circuits part of the exam some useful equations and transforms are provided.

8. All questions are of equal value. Part Marks will be given for right procedures.

Front Page

16-MEX-A2

PART A

CIRCUITS

ANSWER A MAXIUM OF 3 QUESTIONS FROM THIS PART A SECTION AND TWO QUESTIONS FROM THE PART B SECTION

OR

ANSWER 2 QUESTIONS FROM THIS PART A SECTION AND 3 QUESTIONS FROM THE PART B SECTION

Q1: For the circuit shown in Figure-1,

(a) Calculate the equivalent resistance of the circuit , R_{AB} at the terminals A and B. [10]

(b) Solve for the current I at the location shown. [5]

(c) Calculate the Power dissipation in the 12Ω resistance. [5]

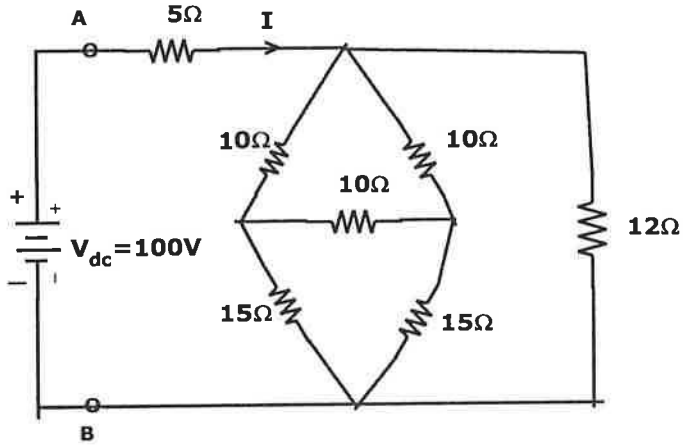


Figure-1

Q2: In the Figure-2 solve the voltage, V_o by the Superposition theorem. [20]

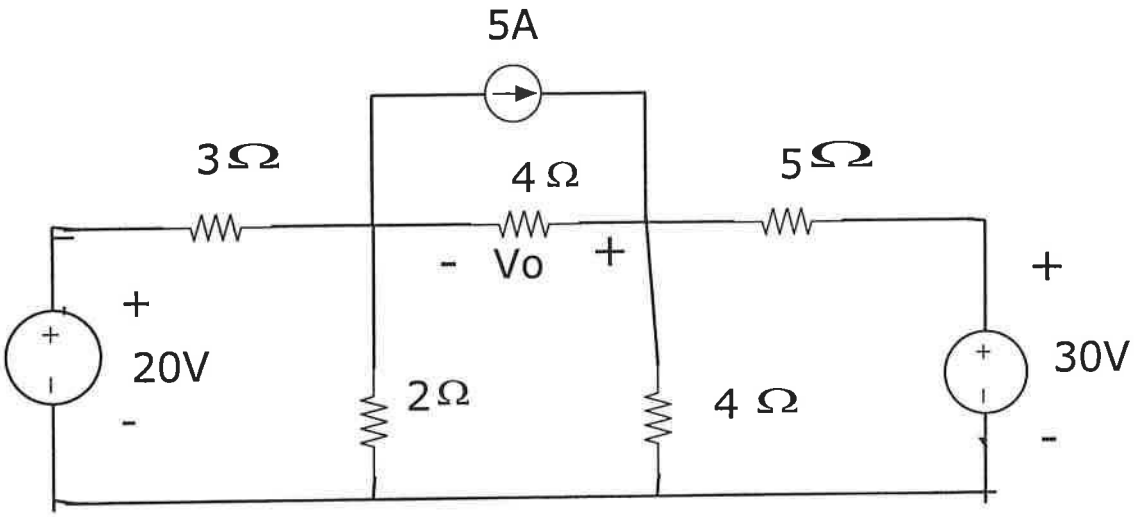


Figure-2

Q3: In Figure-3, the switch was in position-A for a long time. At t = 0, it is moved to Position-B.

Calculate (i) $v_c(0+)$, $\frac{dv_c}{dt}(0+)$, and $v_c(\infty)$ [4+6+2]

(ii) $v_c(t)$ when $t \geq 0$ [8]

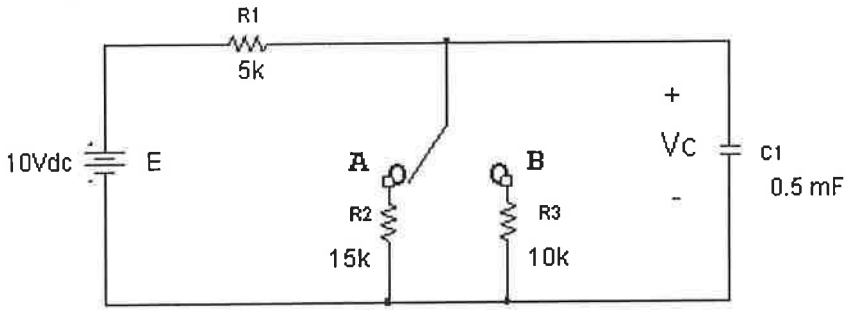


Figure-3

Q4: **(a)** For the circuit shown in Figure-4, calculate the load resistance R_L to be connected across the terminals a and b for maximum power dissipation. [10]

(b) Calculate this maximum possible power dissipation in R_L. [10]

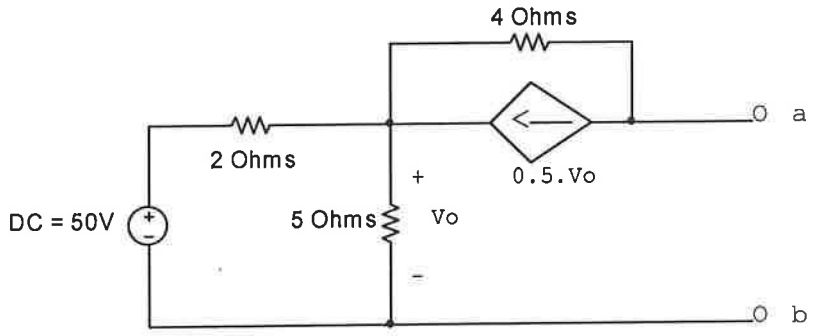


Figure-4

Q5: (a) Write the Node Voltage equations of the following ac circuit, Figure-5, where the frequency is 60 Hz. [8]

(b) Solve the node voltages, and calculate the power supplied by the voltage source, e. [6+6]

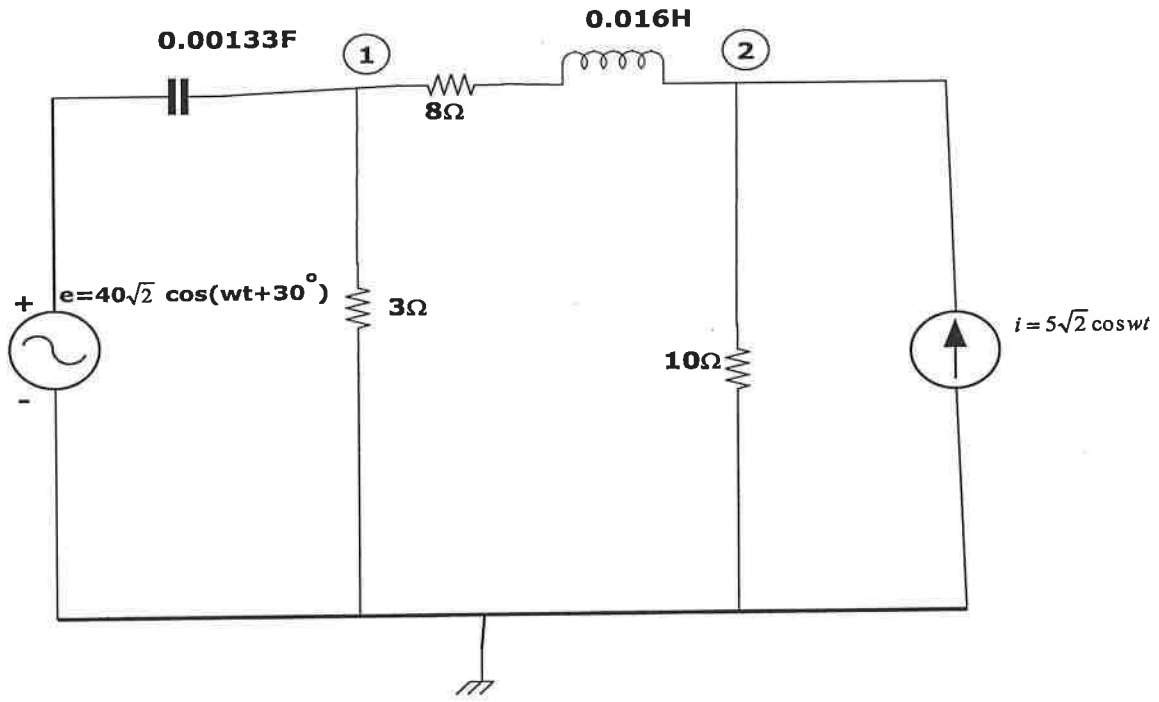


Figure-5

Q6: (a) In the circuit shown in Figure-6, the switch was on position-a for a long time. At t = 0, the switch is moved to position-b. Calculate $V_c(0^+)$ and $i(0^+)$. [4]

(b) Draw the Laplace Transformed circuit at $t \geq 0$. [8]

(c) Solve $V_c(t)$. [8]

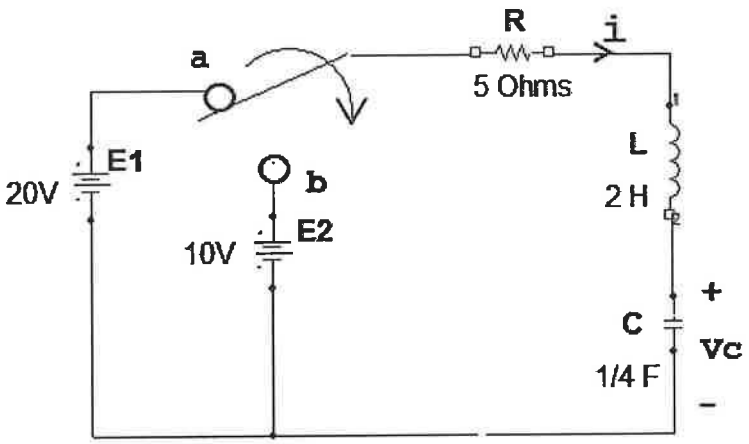


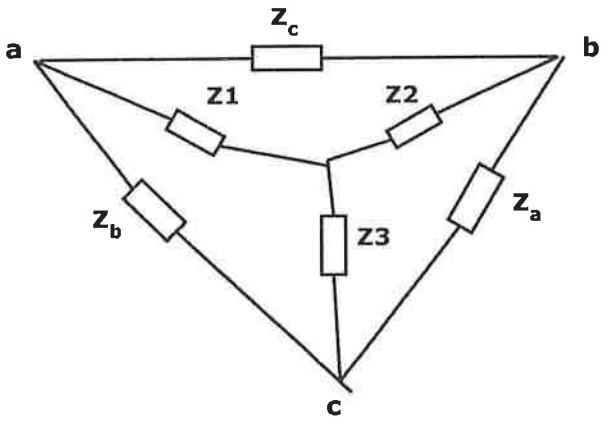
Figure-6

Appendix

Some useful **Laplace Transforms:**

f(t)	→	F(s)
Ku(t)		K /s
$\partial(t)$		1
t		$1/s^2$
e^{-at} u(t)		1 / (s+a)
sin wt .u(t)		$w / (s^2+w^2)$
cos wt . u(t)		$s / (s^2+w^2)$
$e^{-\alpha t} \sin \omega t$		$\frac{\omega}{(s+\alpha)^2+\omega^2}$
$e^{-\alpha t} \cos \omega t$		$\frac{(s+\alpha)}{(s+\alpha)^2+\omega^2}$
$\frac{df(t)}{dt}$		$s F(s) - f(0^-)$
$\frac{d^2 f(t)}{dt^2}$		$s^2F(s) - s f(0^-) - f^1(0^-)$
$\int_{-\infty}^{t} f(q)dq$		$\frac{F(s)}{s} + \int_{-\infty}^{0} f(q)dq$

Star – Delta conversion:



$$Z_1 = \frac{Z_b . Z_c}{Z_a + Z_b + Z_c} \qquad Z_2 = \frac{Z_a . Z_c}{Z_a + Z_b + Z_c} \qquad Z_3 = \frac{Z_a . Z_b}{Z_a + Z_b + Z_c}$$

$$Z_a = \frac{Z_1 . Z_2 + Z_2 . Z_3 + Z_3 . Z_1}{Z_1} \qquad Z_b = \frac{Z_1 . Z_2 + Z_2 . Z_3 + Z_3 . Z_1}{Z_2}$$

$$Z = \frac{Z_1 . Z_2 + Z_2 . Z_3 + Z_3 . Z_1}{Z_3}$$

16-MEX-A2

PART B

ELECTRONICS

ANSWER A MAXIUM OF 3 QUESTIONS FROM THIS PART B SECTION AND TWO QUESTIONS FROM THE PART A SECTION

OR

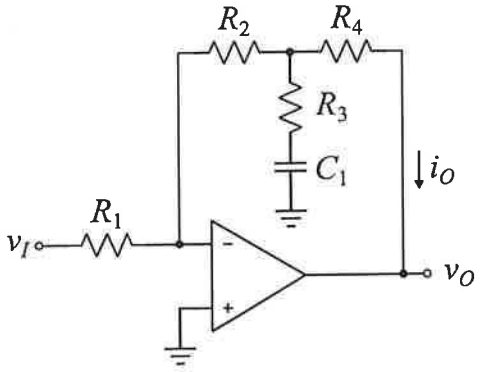
ANSWER 2 QUESTIONS FROM THIS PART B SECTION AND 3 QUESTIONS FROM THE PART A SECTION

QUESTION (7)

The op amp in the following circuit is ideal except for an input offset voltage of ±3 mV.

a) What is the output DC offset voltage? (8 point)

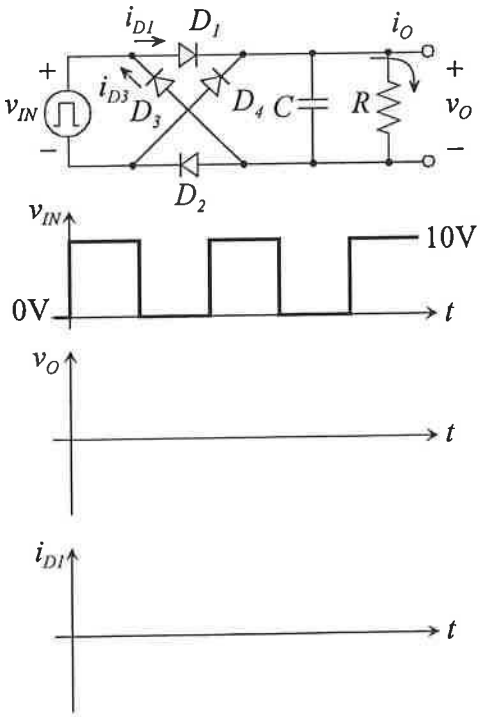
b) What is the small signal voltage gain v_O/v_I? (12 point)



Given: $R_1 = R_2 = R_4 = 100\ \text{k}\Omega$
$R_3 = 1\ \text{k}\Omega$
C_1 = very large

QUESTION (8)

The diodes are ideal except with an on-voltage of 0.7V. The input voltage source v_{IN} is a 100Hz, 50% duty cycle square-wave with voltage levels of 0V and +10V. The load resistance, $R = 100\Omega$.



a) If the ripple voltage, $V_r = 0.5$V, sketch the output waveform for several input cycles. What is the average DC output voltage v_O. (6 points)

b) What would be the minimum value of C (in μF) required to keep $V_r \leq 0.5$V ? (4 points)

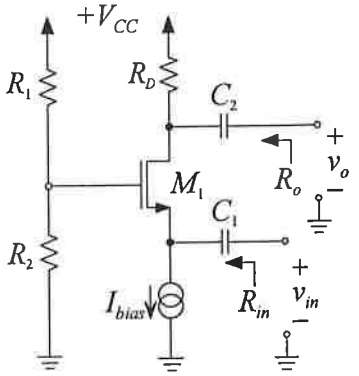
c) Sketch the current waveform for i_{D1} flowing through diode D_1. Indicate the time interval that the capacitor is charging. (6 points)

d) What is the overall average current (i_{D3}) flowing through diode D_3? (4 points)

QUESTION (9)

Transistor M_1 in this common gate amplifier circuit has the following characteristics:

$V_{TH} = 1$ V
$K = 1$ mA/V^2 $\lambda = 0.1$



Given: $V_{DD} = 10$ V, $I_{bias} = 2$ mA,
$C_1 = C_2 = \infty$,
$R_1 = 10$ kΩ, $R_2 = 5$ kΩ, $R_D = 2$ kΩ

a) Determine the small signal gain, v_o/v_{in}. (12 points)

b) Determine the input resistance, R_{in}. (4 points)

c) Determine the output resistance, R_o. (4 points)

Useful formulae: for n-channel MOSFET

$$i_{DS} = K\left[(v_{GS} - V_{TH})v_{DS} - \frac{1}{2}v_{DS}^2\right] \quad \text{triode region}$$

$$i_{DS} = \frac{1}{2}K(v_{GS} - V_{TH})^2(1 + \lambda v_{DS}) \quad \text{saturation region}$$

QUESTION (10)

This is an enhancement load NMOS inverter. Given that the transistors are identical,

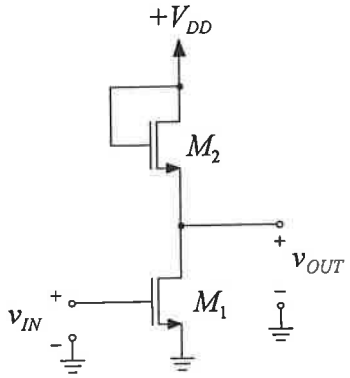
a) Draw the input to output voltage transfer characteristic (VTC) for this inverter. Express and label clearly all voltage levels on the VTC plot. (12 points)

b) Indicate the noise margins NM_L and NM_H on the VTC. (2 points)

c) Indicate the logic high and low output voltage levels V_{OH}, V_{OL} on the VTC. (2 points)

d) Indicate the logic high and low input voltage levels V_{IH}, V_{IL} on the VTC. (2 points)

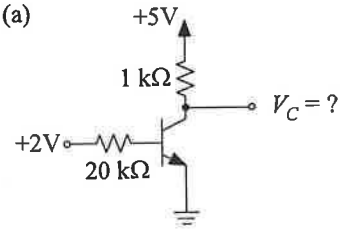
e) Indicate clearly the mode of operation for transistors M_1 and M_2 in each region of the VTC. (2 points)



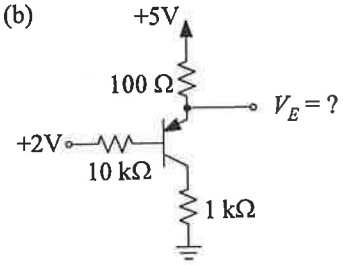
QUESTION (11)

In this question, all BJT transistors have $\beta = 50$, $V_{BE,on}$ or $V_{EB,on} = 0.6V$, $V_{CE,sat}$ or $V_{EC,sat} = 0.3V$ and $V_A = \infty$. Solve for the required voltages. (20 points)

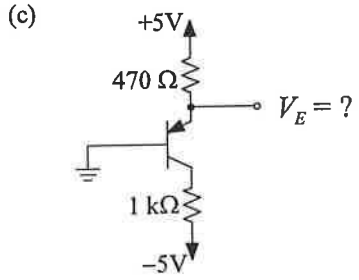
(a) (4 points)



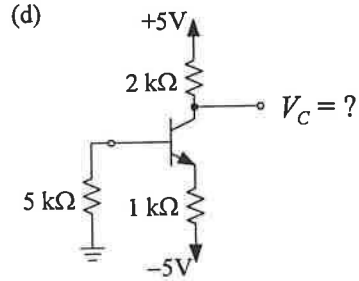
(b) (4 points)



(c) (4 points)



(d) (4 points)



(e) (4 points)