National Exams

98-Comp-A3, Computer Architecture

3 hours duration

NOTES:

1. If doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumptions made.

2. This is an OPEN BOOK EXAM.
   Any non-communicating calculator is permitted.

3. FIVE (5) questions constitute a complete exam paper.
   The first five questions as they appear in the answer book will be marked.

4. Each question is of equal value.

5. Most questions require an answer in essay format. Clarity and organization of the answer are important.

Marking Scheme

1. (a) 10 marks (b) 5 marks (c) 5 marks
2. (a) 10 marks (b) 10 marks
3. (a) 5 marks (b) 10 marks (c) 5 marks
4. (a) 5 marks (b) 5 marks (c) 10 marks
5. 20 marks
6. (a) 5 marks (b) 10 marks (c) 5 marks

1. **(a)** A simple processor has a memory address space of 32Kwords. Its memory is word addressable. **All** instructions take the form:

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   OP Destination, Source, nextPC
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   Destination, Source, and nextPC are word addresses in memory and OP is some operation to be performed. If every instruction is represented using 64 bits, how many different instructions can this processor have? Explain your answer.

   (b) Some instruction set architectures use a fixed-instruction length whereas others do not. For example, in some architectures all instructions are 32-bits long whereas in others an instruction may be anywhere from one to 17 bytes long. List the advantages and disadvantages of each approach.

   (c) A processor has a 4GB byte-addressable address space. The 32-bit value at address 0x0400 0000 is 0x1ABCDEF0. Can this be an instruction? Can it be data? Explain your answer.

2. **(a)** An array has 256 elements each of two bytes. Assuming that the first element of the array appears at address BASE, where in memory will the N-th element of the array be? Assume a byte-addressable memory address space.

   (b) A processor has a 4GB byte-addressable address space. The processor uses the big-endian convention for storing memory values. The elements of a linked list contain each a single 4-byte integer plus a pointer to the next element in the list. Show how the following linked list will be stored in memory: (1)-->(2)-->(3). Where (1) represents an element storing the value 1, and (1)-->(2) shows that the element storing the value 1 points to the element storing the value 2. Show the exact contents of memory for all three elements assuming that the element (1) is stored starting at address 0x100, followed by the element (2) and element (3) in that order.

3. **(a)** A processor has a 4GB byte-addressable address space. How will a 32KB, 2-way set-associative cache with 64-byte blocks be indexed. Explain your answer.

   (b) Assuming that a cache's total capacity remains constant how will its hit rate vary as a function of its block size? Draw a diagram with the block size along the x-axis and show a curve for the expected behavior for the miss rate. Explain your answer for what is the expected behavior.

(c) The primary purpose of a cache is to reduce the average access latency for memory operations. Does a cache always improve performance? Explain your answer.

4. (a) What are caller-saved and what are callee-saved registers. When is it better to use one over the other?

   (b) Some architectures pass all function call arguments through the stack while others pass some of the arguments through registers. What can be the advantages of the second method? Is it possible to pass all arguments through registers?

   (c) Given two unsigned integer values A and B, is the following always true in a modern processor? A + B > A. How about A – B < A? Explain your answer.

5. A multiple cycle implementation of a processor requires 6 cycles for the LI instruction, 5 cycles for all ARITHMETIC instructions and the MEMORY READ instruction, and 4 cycles for the MEMORY STORE and BRANCH instructions. No other instructions exist. The implementation can be modified so the LI instruction requires 5 cycles instead but at the expense of reducing the clock frequency by 5%.

   On the average, programs execute instructions with the following frequency:

LI	10%
ARITHMETIC	50%
MEMORY READ	20%
MEMORY STORE	10%
BRANCH	10%

   Which implementation (original or modified) will execute programs faster and by how much assuming the aforementioned mix of instructions? Explain your answer.

6. (a) A memory chip has the following interface: A0-A14 are 15 single bit input address lines specifying which row is accessed, a single bit input signal R/W! specifies whether the access is a read (1) or a write (0), E is a single bit input signal that must be 1 to access the chip. The data values that are read or written appear on the four D3-D0 single bit output/input pins. When E is 0 the D3-D0 pins are in high-Z. What is the total capacity of this memory chip in bytes?

(b) Using as many as necessary of the chips described in part (a), synthesize the equivalent of an 8-bit wide chip that has a 64KB total capacity. You can use a few additional logic gates as needed.

(c) A memory interface has the following signals: L0-L31 are 32 single-bit output address lines specifying which memory location is accessed, a single bit output ME signal is 1 when an access is taking place, a single bit R/W! output signal is 1 or 0 for reads and writes respectively, D0-D7 are eight single-bit bi-directional data signals that either provide the value to be written or expect the value to be read. Connect a 64KB chip with the interface described in part (b) to this memory interface. The chip should be activated for accesses in the range of 0x10000 – 0x1FFFF.