National Exams May 2016

04-BS-8, Digital Logic Circuits

3 hours duration

NOTES:

1. If a doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumption made with the answer of the question.

2. Candidates may use one of two calculators, the Casio or Sharp approved models. This is a closed book examination; however, candidates are allowed to bring one hand-written information sheet (8.5" X 11") of self-prepared notes.

3. This paper contains **FIVE (5)** questions and comprises **SIX (6)** pages.

4. Any **FOUR (4)** questions constitute a complete paper. Only the first four questions as they appear in your answer book will be marked.

5. All questions are of equal marks. Total marks = 100.

6. Each question carries 25 marks and the marks for each part of the question are indicated in brackets.

7. Some relevant Data sheets are provided in Appendix at the end of paper.

1. (a) Identify the main differences between PAL, ROM and FPGA devices that are used to implement digital logic circuits.

   (6 marks)

   (b) Design and implement a digital circuit using minimum number of 2-input NAND gates only. The circuit has four inputs (w, x, y and z) and three outputs (F1, F2 and F3). F1, F2 and F3 outputs are represented by following Boolean expressions.
   $$F1(w, x, y, z) = \sum m(0, 2, 4, 6, 7, 9, 11, 13)$$
   $$F2(w, x, y, z) = \sum m(0, 1, 4, 6, 8, 10, 14)$$
   $$F3(w, x, y, z) = \sum m(1, 3, 4, 7, 9, 12, 15)$$

   Show your complete work based on K-map based simplification and your overall circuit design must employ minimum number of 2-input NAND gates.

   (12 marks)

   (c) Implement the Boolean function, $F2(w, x, y, z)$ in part (b) by using a 3-to-8 decoder (given in Appendix) along with minimum number of gates.

   (7 marks)

2. Design a clocked synchronous finite state machine with one input X, and one output Z. The output is asserted (for one clock cycle) whenever the input sequence (serial data) ...0110... has been observed, as long as the sequence ...1000... has never been observed.

   A typical sample of the input data X, and output Z are given below (note the position of Z assertions):

   X: 0110011011011011101101101000110100000...
   Z: 0000100010010010000000100000000000000 ...

   (a) Draw the state diagram of the finite state machine with minimum number of states.

   (10 marks)

   (b) Design and implement the synchronous finite state machine by using flip-flops and logic gates of your choice.

   (15 marks)

3. Provide a brief answer or draw the circuit for the following questions with justification.

(a) Design a D-type flip-flop by using a SR flip-flop and other logic gates. Draw the complete logic diagram of the circuit.

(5 marks)

(b) If A = 1, B = 0, and C = 1, then find **X,** where **X** = ($\overline{A \oplus B}$) . C

(4 marks)

(c) Identify the clocked flip-flop described in the following characterization table.

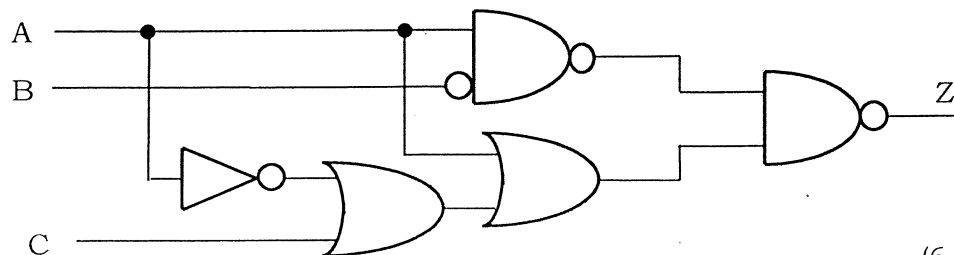| Inputs A	B	Output Qn+1
0	0	Qn
1	0	0
0	1	1
1	1	$\overline{Qn}$

(5 marks)

(d) Considering a 4-Kbyte size memory that facilitates a byte-wide read and identify, which of the following information is correct:
   i). 4000 address lines and 32 data lines.
   ii). 14 address lines and 8 data lines.
   iii). 12 address lines and 8 data lines.
   iv). 10 address lines and 8 data lines.

Justify your answer.

(5 marks)

(e) Determine the Boolean expression for output Z of the circuit given below. Simplify the Boolean expression using Boolean algebra.

(6 marks)

4. (a) A sequence controller is being developed to simulate a traffic light system. The controller has three active-low TTL outputs that drive green, yellow and red LEDs respectively. The LEDs emulate the following traffic light sequence repeatedly:
   - Green LED on for 24 seconds.
   - Both Yellow and Green LEDs on for 4 seconds.
   - Red LED on for 28 seconds

   Design the controller by using a suitable size counter and some other logic. Assume that a clock signal of 0.25 Hz is available. Draw the timing diagrams for signals driving the Green, Yellow and Red LEDs. Show your complete design of the sequence controller.

   (19 marks)

   (b) Is it possible to design the part (a) controller circuit by using a shift register? If yes what will be the size of the shift register. Justify your answer.

   (6 marks)

5. (a) List any difference between sign-magnitude and 2's complement representations. Describe any advantage of each of the representations.

   (6 marks)

   (b) Identify the difference between ripple-carry and carry look-ahead adder circuits. Describe any reason why a ripple-carry adder takes more time to add as compared to a carry look-ahead adder.
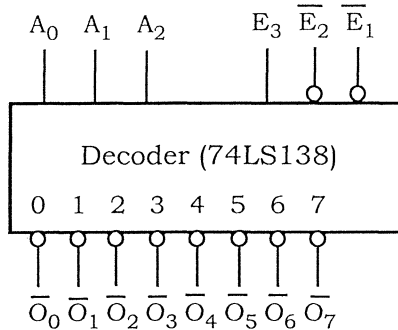
   (7 marks)

   (c) Design and implement a 4-bit ripple-carry adder by using minimum number of 2-input AND, OR and XOR gates.
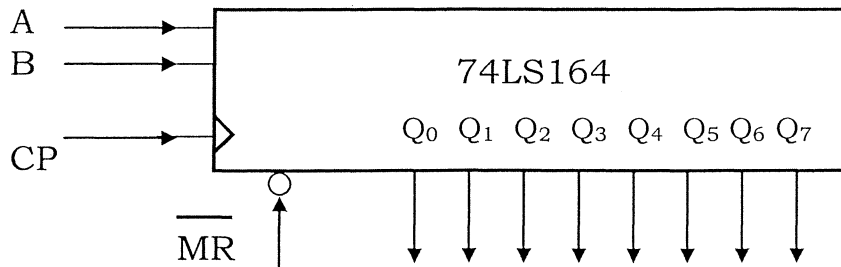
   (12 marks)

APPENDIX

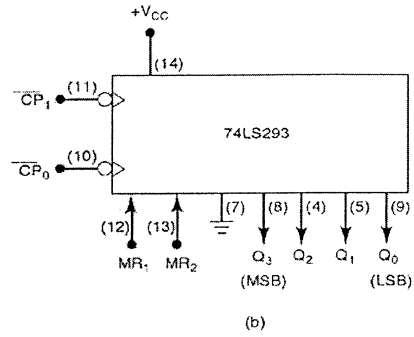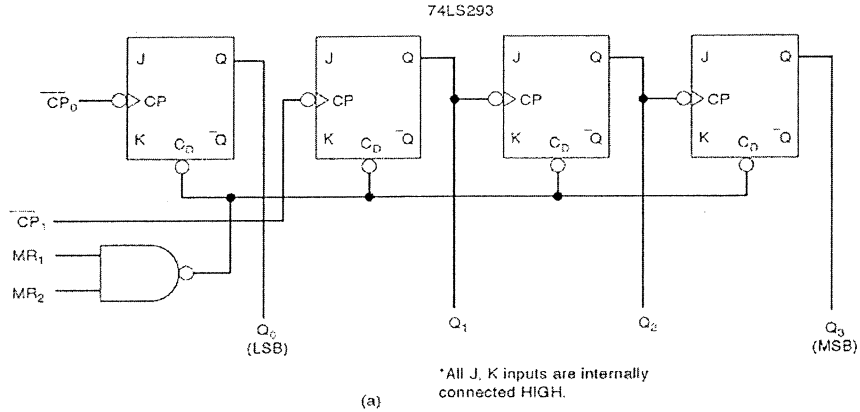## Decoder, Counter & Shift Register Data Sheets

74LS138: 3-to-8 Decoder

Inputs			Outputs
$\overline{E_1}$	$\overline{E_2}$	E_3	
0	0	1	Respond to input code $A_2 A_1 A_0$
1	x	x	Disabled - all HIGH
x	1	x	Disabled - all HIGH
x	x	0	Disabled - all HIGH

74LS164: 8-bit Shift Register

- An eight-bit shift register with all FF outputs Q_0, Q_1, Q_2, Q_3, Q_4, Q_5, Q_6 and Q_7 are externally available.
- Inputs A and B are ANDED together to produce the serial input to flip-flop Q_0.
- Shift operation occurs at PGTs of the clock input CP.
- The $\overline{MR}$ input resets all FFs asynchronously on a LOW level.

74LS293 : 3/4-bit counter

74LS293

*All J, K inputs are internally
connected HIGH.

(a)

(b)

END OF Paper