National Exams May 2019

17-Comp-A1, Electronics

3 hours duration

NOTES:

1. If doubt exists as to the interpretation of any question, the candidate is urged to indicate, with the answer, a clear statement of any assumptions made.

2. This is an OPEN BOOK exam.
   Any non-communicating calculator is permitted.

3. FIVE (5) questions constitute a complete exam paper.
   The first 5 questions as they appear in the answer book will be marked.

4. Each question is of equal value.

Marking Scheme

1. 20 marks total (4 parts, 5 marks each)
2. 20 marks total (3 parts, a)7 marks, b)7 marks, c) 6 marks)
3. 20 marks total (4 parts, 5 marks each)
4. 20 marks total (4 parts, 5 marks each)
5. 20 marks total (3 parts, a) 6 marks, b) 7marks, c) 7 marks)
6. 20 marks total (4 parts, 5 marks each)
7. 20 marks total (4 parts, 5 marks each)

Question 1 (20 marks)

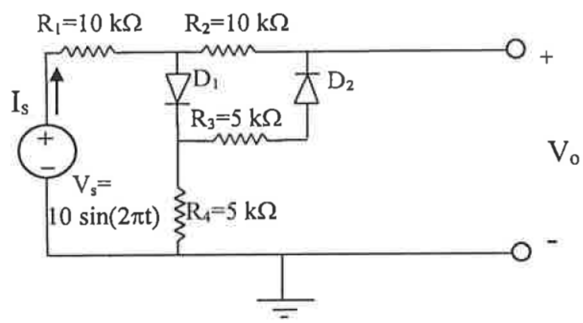

Figure 1. All diodes have a forward voltage drop V_D=0.7V.

The circuit shown in Figure 1 is in steady state:

a) Sketch V_S and V_o as a function of time, indicating peak voltages.
b) What maximum reverse voltage rating would you choose for the diodes?
c) Which resistor has the largest peak power dissipation? What power rating would you choose for this resistor?
d) Sketch current I_S as a function of time, indicating peak values.

Question 2 (20 marks)

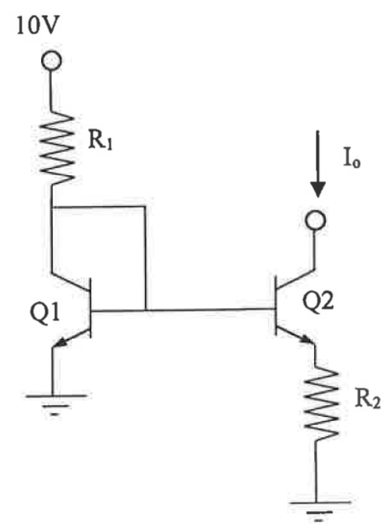

Figure 2. V_{BE}=0.7V for I_C=1mA, β=100, V_T=25mV, V_A=100V.

For the circuit shown in Figure 2:

a) Choose R_1 and R_2 so I_o is 100 μA
b) Find the small signal output resistance of the circuit.
c) If R_2=0Ω, repeat a) and b).

Question 3 (20 marks)

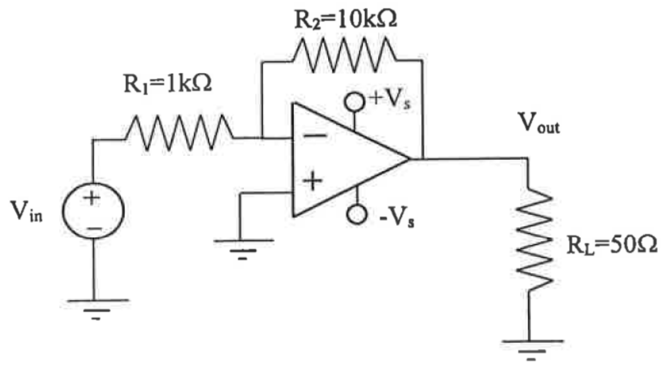

Figure 3. $+V_s$=15V, $-V_s$=-15V, I_s=100mA from each supply, V_{in}=1V@1kHz.

For the circuit shown in Figure 3:

a) Find voltage gain $|A_v|$ and power gain $|A_p|$ in dB
b) Find the efficiency of the amplifier
c) Draw an equivalent circuit for the amplifier including component values
d) What is the maximum input possible without clipping of the output waveform?

Question 4(20 marks)

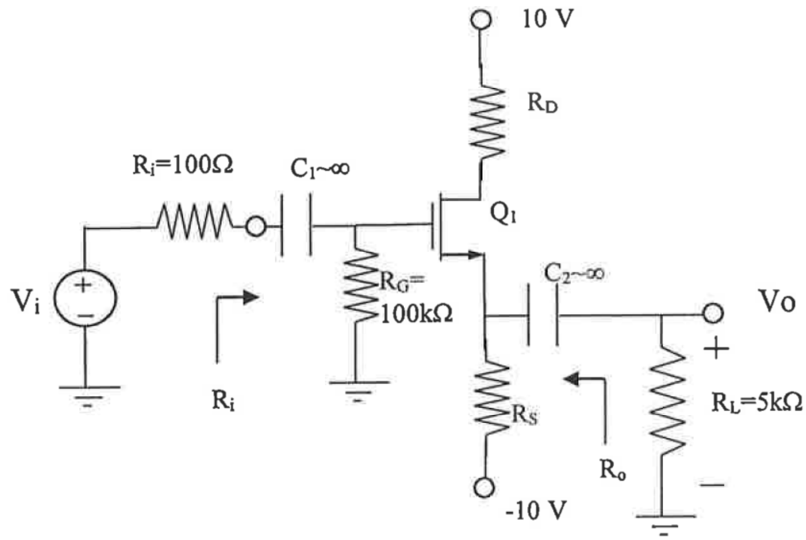

Figure 4. $k_n'(W/L)=0.5mA/V^2$, $V_t=2V$, $V_A=50V$

For the circuit shown in Figure 4:

a) Choose values for R_D and R_S to provide $I_D=1mA$.
b) Draw a small signal equivalent circuit and evaluate the model parameter values.
c) Find the small signal input resistance R_i and output resistance Ro.
d) Find the voltage gain for the amplifier.

Question 5 (20 marks)

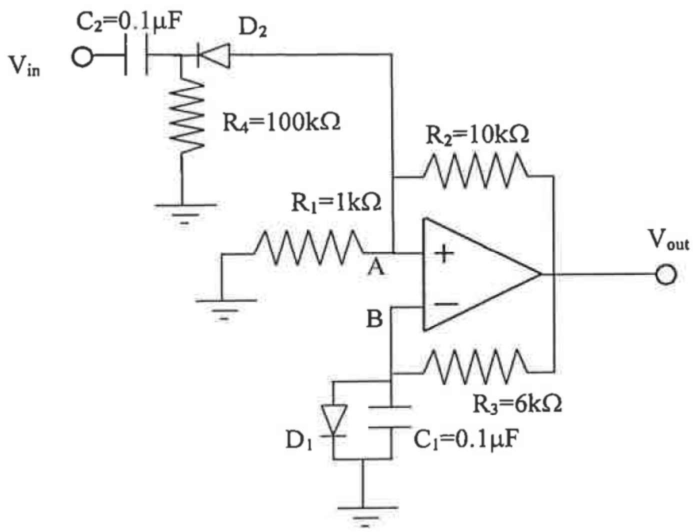

Figure 5.

The circuit shown in Figure 5 is in steady state with V_{in}=0V for t<0. At t=0 V_{in} drops to -5V. All diodes have a forward voltage drop V_D=0.7V. The amplifier is supplied +/-12 V.

a) For t<0 explain the expected steady state value for V_{out}.
b) For t>0 explain the circuit operation
c) For t>0 sketch V_{out} ,V_A and V_B as a function of time including key amplitude and time values.

Question 6 (20 marks)

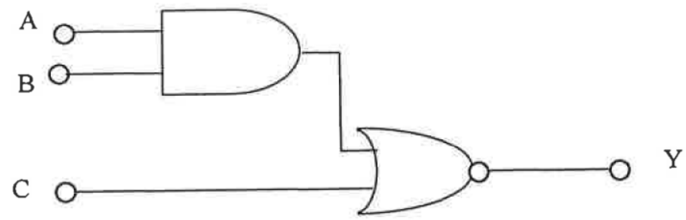

Figure 6.

Consider a CMOS technology with C_{ox}=1fF/μm^2, $\mu_n C_{ox}$=50μA/V^2, $\mu_p C_{ox}$=20μA/V^2, V_{tn}=-V_{tp}=1V, and V_{DD}=5V. An inverter with a minimum gate length L=0.5 μm has a symmetric transfer function for NMOS W/L = 1.5 and PMOS W/L =6.

a) Provide a Boolean expression for Y based on the gate combination shown in Figure 6.
b) Synthesize a transistor level CMOS logic circuit to implement this expression.
c) Specify sizes (W/L) for all transistors in order to achieve current-driving capability equal to that of the basic inverter.
d) If the output Y drives a standard inverter in this technology, evaluate the propagation delays considering only the inverter gate capacitance as a load.

Question 7 (20 marks)

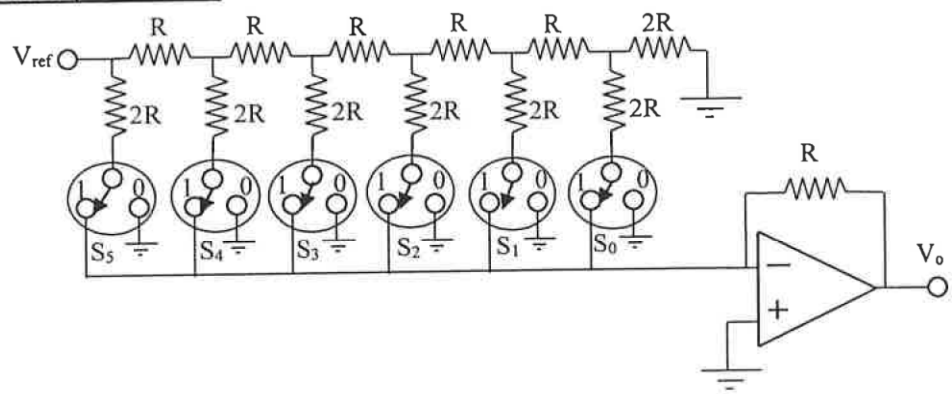

Figure 7. R=10kΩ, V_{REF}=2.5V. Switches hold the position shown if the control voltage is high, and connect to ground if the control voltage is low.

a) Evaluate the current through each switch if the control signal S=(111111)

b) Evaluate the current through each switch if the control signal S=(000000)

c) Evaluate the output voltage for S=(001001).

d) Describe another approach to implement the function of this circuit.