National Exams May 2017

04-BS-8, Digital Logic Circuits

3 hours duration

NOTES:

1. If a doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumption made with the answer of the question.

2. Candidates may use one of two calculators, the Casio or Sharp approved models. This is a closed book examination; however, candidates are allowed to bring one hand-written information sheet (8.5" X 11") of self-prepared notes.

3. This paper contains **FIVE (5)** questions and comprises **FIVE (5)** pages.

4. Any **FOUR (4)** questions constitute a complete paper. Only the first four questions as they appear in your answer book will be marked.

5. All questions are of equal marks. Total marks = 100.

6. Each question carries 25 marks and the marks for each part of the question are indicated in brackets.

1. (a) Identify the main architectural features of FPGA devices that make these devices versatile when compared with PLD (PLA, PAL, etc.) devices used to implement digital logic circuits.

(7 marks)

(b) Design and implement a digital circuit that converts 4-bit sign-magnitude represented integers (ranging from -7 to +7) to 4-bit 2's complement representation. The circuit has four inputs (a3, a2, a1, a0) and four outputs (Z_3, Z_2, Z_1, Z_0).

Show your complete work including the truth table. K-map based simplification and your overall circuit design must employ minimum number of 2-input gates.

(18 marks)

2. Design a clocked synchronous finite state machine with one input A, and one output X. The output is asserted (for one clock cycle) whenever the input sequence (serial data) ...0101... has been observed, as long as the sequence ...1100... has never been observed.

A typical sample of the input data A and output X are given below (note the position of X=1 assertions):

A: 0101000101011010101101100010101010110000...
X: 0000100000100000010000000000000000000000...

(a) Draw the state diagram with minimum number of states.

(9 marks)

(b) Design and implement the synchronous finite state machine by using D-type flip-flops and logic gates of your choice.

(16 marks)

3. Provide a brief answer or draw the circuit for the following questions with justification.

(a) Design a D-type flip-flop by using a JK flip-flop and other logic gates. Draw the complete logic diagram of the circuit.

(4 marks)

(b) If A = 1, B = 0, and C = 1, then find **X**, where $\mathbf{X} = \overline{(A \oplus B)} + A \cdot C$

(4 marks)

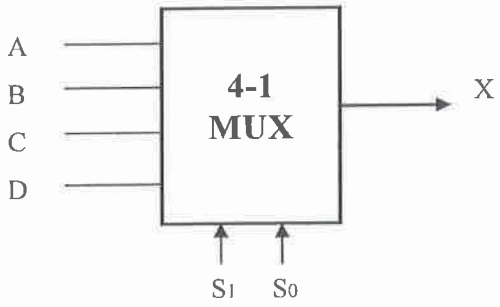
(c) Identify the clocked flip-flop described in the following characterization table. Justify your answer.

Inputs A	Inputs B	Output Qn+1
0	0	Qn
1	0	0
0	1	1
1	1	x

where x is the indeterminate value.

(5 marks)

(d) Consider a 4-to-1 MUX that has four single-bit inputs (A, B, C, D), an output X and two control inputs S_1 and S_0 as given below. The 4-1 MUX is implemented by using 2-6 input AND & OR gates.



Determine the minimum number of AND gates as well as OR gates used to implement the above MUX. Justify your answer by drawing its logic diagram showing all the gates used.

(12 marks)

4. Synthesize and analyze the counter circuit of Figure Q4, where the AND gate is used to detect a particular state of the circuit.

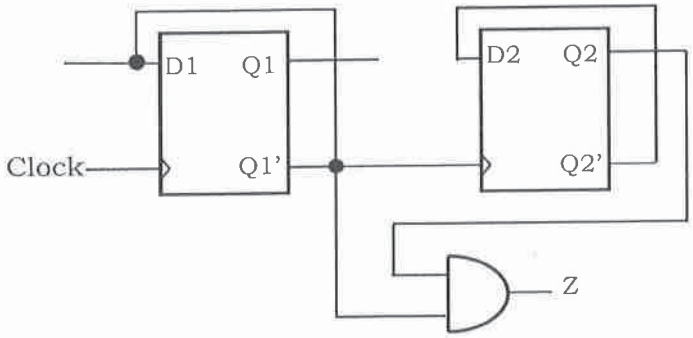


Figure Q4

(a) Is the above circuit a synchronous sequential circuit? (Yes or No) Justify you answer.

(5 marks)

(b) Identify the circuit state that is detected by the AND gate in the above circuit.

(5 marks)

(c) Draw the waveforms of outputs Q1, Q2 and Z for a 10 MHz clock. Assume that both flip-flops are initially reset to 0 and the propagation delay of a flip-flop and the AND gate is 10 ns and 5 ns respectively.

(15 marks)

5. Consider a Boolean function **F** given below.

$$\mathbf{F}(p, q, r) = \mathbf{(p + q + r) \cdot (p + q + r') \cdot (p + q' + r) \cdot (p' + q' + r)}$$

(a) Use Boolean algebraic manipulation to find the minimum product-of-sum expression of function **F.** Implement the function using the minimum number of gates.

(9 marks)

Question No. 5 continues on Page 5

(b) Implement the function **F** by employing the minimum number of AND gates and only one OR gate.

(10 marks)

(c) Implement the minimized form of **F** obtained in part (a) by using only 2-input NAND gates.

(6 marks)

(End OF Paper)