National Exams December 2018

16-Elec-A5, Electronics

3 hours duration

Notes:

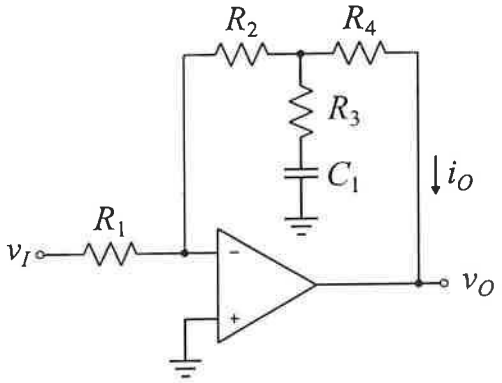
1. If any doubt exists as to the interpretation of any question, the candidate is urged to submit, within their answer, a clear statement of any assumptions made.
2. This is a **CLOSED BOOK EXAM**.
   Approved Casio or Sharp calculator is permitted.
3. Answer all **FIVE** (5) questions.
4. All questions are worth 20 marks each.
5. Please start each question on a new page and clearly identify the question number and part number, e.g. Q4(a).
6. In schematics, ground and chassis may be assumed to be common, unless specifically stated otherwise.
7. Unless otherwise specified, assume that Op-Amps are ideal and that supply voltages are ±15V.
8. If questions require an answer in essay format, clarity and organization of the answer are important. Provide block diagrams and circuit schematics whenever necessary.

QUESTION (1)

The op amp in the following circuit is ideal except for an input offset voltage of ±3 mV.

a) What is the output DC offset voltage? (8 point)

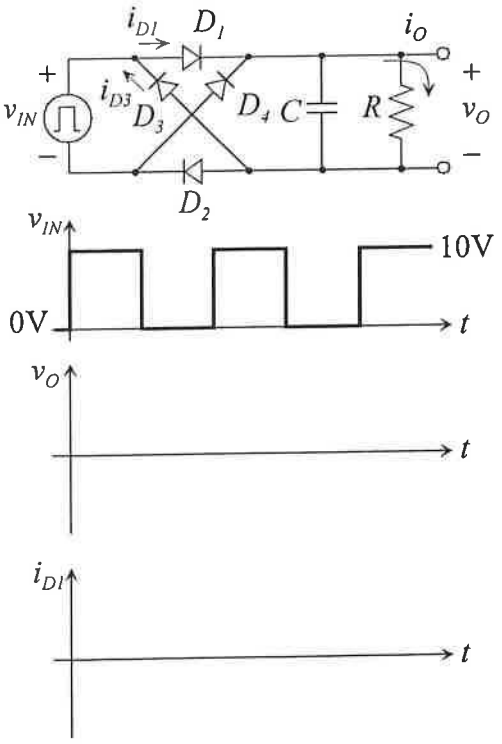
b) What is the small signal voltage gain v_O/v_I? (12 point)



Given: $R_1 = R_2 = R_4 = 100\ \text{k}\Omega$
$R_3 = 1\ \text{k}\Omega$
C_1 = very large

QUESTION (2)

The diodes are ideal except with an on-voltage of 0.7V. The input voltage source v_{IN} is a 100Hz, 50% duty cycle square-wave with voltage levels of 0V and +10V. The load resistance, $R = 100\Omega$.



a) If the ripple voltage, $V_r = 0.5\text{V}$, sketch the output waveform for several input cycles. What is the average DC output voltage v_O. (6 points)

b) What would be the minimum value of C (in μF) required to keep $V_r \leq 0.5\text{V}$? (4 points)

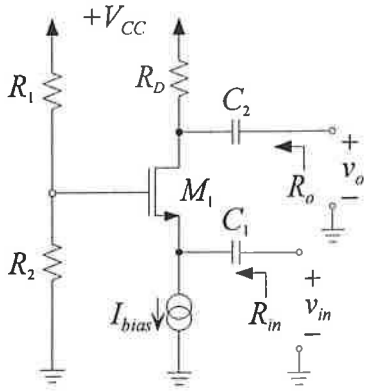
c) Sketch the current waveform for i_{D1} flowing through diode D_1. Indicate the time interval that the capacitor is charging. (6 points)

d) What is the overall average current (i_{D3}) flowing through diode D_3? (4 points)

QUESTION (3)

Transistor M_1 in this common gate amplifier circuit has the following characteristics:

$V_{TH} = 1$ V
$K = 1$ mA/V^2 $\lambda = 0.1$



Given: $V_{DD} = 10$ V, $I_{bias} = 2$ mA,
$C_1 = C_2 = \infty$,
$R_1 = 10$ kΩ, $R_2 = 5$ kΩ, $R_D = 2$ kΩ

a) Determine the small signal gain, v_o/v_{in}. (12 points)

b) Determine the input resistance, R_{in}. (4 points)

c) Determine the output resistance, R_o. (4 points)

Useful formulae: for n-channel MOSFET

$$i_{DS} = K\left[(v_{GS} - V_{TH})v_{DS} - \frac{1}{2}v_{DS}^2\right]$$ triode region

$$i_{DS} = \frac{1}{2}K(v_{GS} - V_{TH})^2(1 + \lambda v_{DS})$$ saturation region

QUESTION (4)

This is an enhancement load NMOS inverter. Given that the transistors are identical,

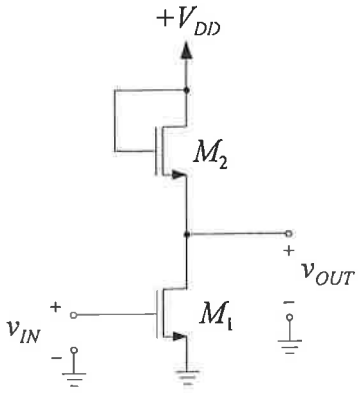
a) Draw the input to output voltage transfer characteristic (VTC) for this inverter. Express and label clearly all voltage levels on the VTC plot. (12 points)

b) Indicate the noise margins NM_L and NM_H on the VTC. (2 points)

c) Indicate the logic high and low output voltage levels V_{OH}, V_{OL} on the VTC. (2 points)

d) Indicate the logic high and low input voltage levels V_{IH}, V_{IL} on the VTC. (2 points)

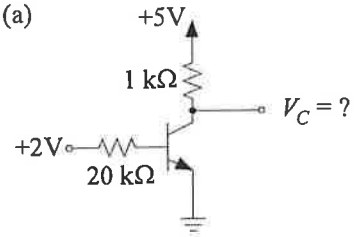
e) Indicate clearly the mode of operation for transistors M_1 and M_2 in each region of the VTC. (2 points)



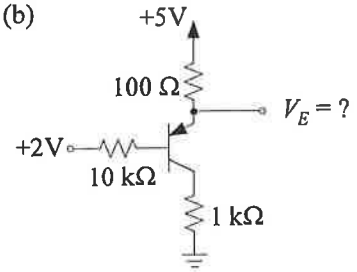
QUESTION (5)

In this question, all BJT transistors have $\beta = 50$, $V_{BE,on}$ or $V_{EB,on} = 0.6V$, $V_{CE,sat}$ or $V_{EC,sat} = 0.3V$ and $V_A = \infty$. Solve for the required voltages. (20 points)

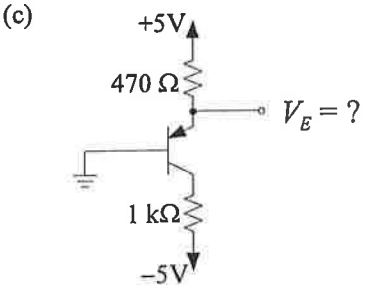
(a) (4 points)



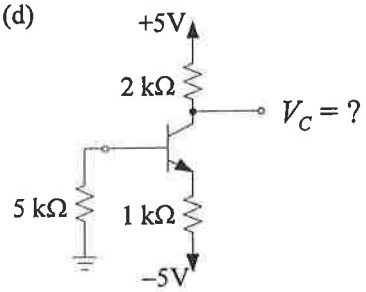
(b) (4 points)



(c) (4 points)



(d) (4 points)



(e) (4 points)