National Exams December 2019

04-BS-8, Digital Logic Circuits

3 hours duration

NOTES:

1. If a doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumption made with the answer of the question.

2. Candidates may use one of two calculators, the Casio or Sharp approved models. This is a closed book examination; however, candidates can bring one hand-written information sheet (8.5" X 11") of self-prepared notes.

3. This paper contains **FIVE (5)** questions and comprises **five (5)** pages.

4. Any **FOUR (4)** questions constitute a complete paper. Only the first four questions as they appear in your answer book will be marked.

5. All questions are of equal marks. Total marks = 100.

6. Each question carries 25 marks and the marks for each part of the questions are indicated in brackets.

7. A PAL16L8 Data sheet is provided in the Appendix. It can be used to provide the solution of Question 4, part (c) and should be attached to your answer sheet.

1. Design a synchronous up-down counter that has the following up and down sequences: (0, 2, 4, 5, 6, and repeat) and (7, 5, 4, 3, 1, and repeat). The counter has a 1-bit control input (C), such that the counter counts upward when C = 0 and counts downward when C =1. Use negative edge triggered D-type flip-flops and logic gates to implement the up-down counter.

(a) Start your design with a state diagram of the up-down counter.

(5 marks)

(b) Develop the next state equations and simplify them if required. Show your complete work.

(12 marks)

(c) Implement and draw the synchronous counter circuit.

(8 marks)

2. Consider a Boolean function **F** given below:

$\mathbf{F}(w,x,y,z) = \mathbf{(w.x.y.z) + (w.x'.y.z) + (w'.x'.y.z') + (w.x.y.z') + (w.x'.y.z')}$

(a) Use Boolean algebra to simplify and find the minimum product-of-sum expression for function **F.** Implement the function using the minimum number of NOR gates only.

(9+5 marks)

(b) Implement the function **F** by employing minimum number of standard gates such as AND, OR and inverter gates.

(5 marks)

(c) Implement the minimized form of **F** in part (a) by using only 2-input NAND gates.

(6 marks)

3. (a) Construct a D-type flip-flop by using a JK flip-flop and minimum number of logic gates. Draw a diagram of the D-type flip-flop.

(5 marks)

(b) If a digital system has 5 inputs, how many possible input combinations are there?

(2 marks)

Question No. 3 continues on Page 3

(c) If A = 0, B = 1, and C = 1; find **X** where $\mathbf{X} = (A \oplus B)' \cdot C$

(2 marks)

(d) Synthesize the following sequential circuit of Figure Q2 and describe the operation of the circuit. Identify the main function of this circuit by providing an example, where the 8-bit shift register is loaded with $(11001110)_2$ and the J-K flip-flop is cleared. Determine the content of the shift register after 8 clock cycles have been applied. You may ignore any propagation delay.

(16 marks)

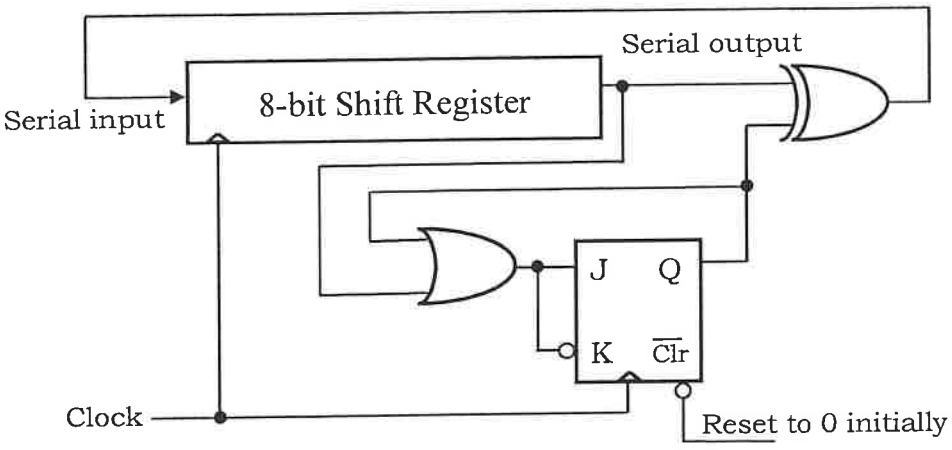


Figure Q3

4. (a) Define Excess-3 (or 10-excess-3 binary) code and identify at least one advantage of employing Excess-3 codes in digital systems.

(6 marks)

(b) Design a digital system that converts a 3-bit BCD number to a 3-bit Excess-3 code. Show your complete system design and implementation by using minimum number of NAND gates only.

(12 marks)

(c) Implement the 3-bit BCD to Ecess-3 code conversion circuit of part (b) by using a PAL16L8 programmable logic. Show the intact PAL fuses by crossing them in the diagram given in the Appendix and attach it to your answer book.

(7 marks)

5. A sequential circuit is required that can generate an even parity for a sequence of 5-bit binary data. The 5-bit binary number is available on a serial input channel. The even-parity generator circuit receives a serial stream of 5-bit number, start Synch pulse and a synchronizing clock from a data system as shown in Figure Q5. The parity generator circuit asserts its even parity output (**even**) for one clock cycle, when it receives the 5-bit number starting with a Synch pulse of one clock cycle duration at the positive transitions of the Clock. The main features of the system are given below:

- Clock signal from the data system unit shifts the data bits in serially.
- Each input bit spans between consecutive negative transitions of the clock.
- The 5-bit serial data starts with its least significant bit.

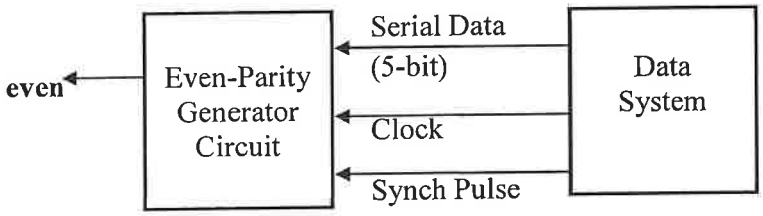


Figure Q5

Design the Parity generator circuit such that its output, **even** is available during the 5th bit of a 5-bit data. The **even** parity bit is set or reset to have an even number of 1's in the 6-bit number (5-bit Data and 1-bit parity).

(a) Draw the state diagram and state table for the even-parity generator sequential circuit.

(7 marks)

(b) Design the parity generator by using a suitable edge-triggered (negative or positive) D-type flip-flops.

(12 marks)

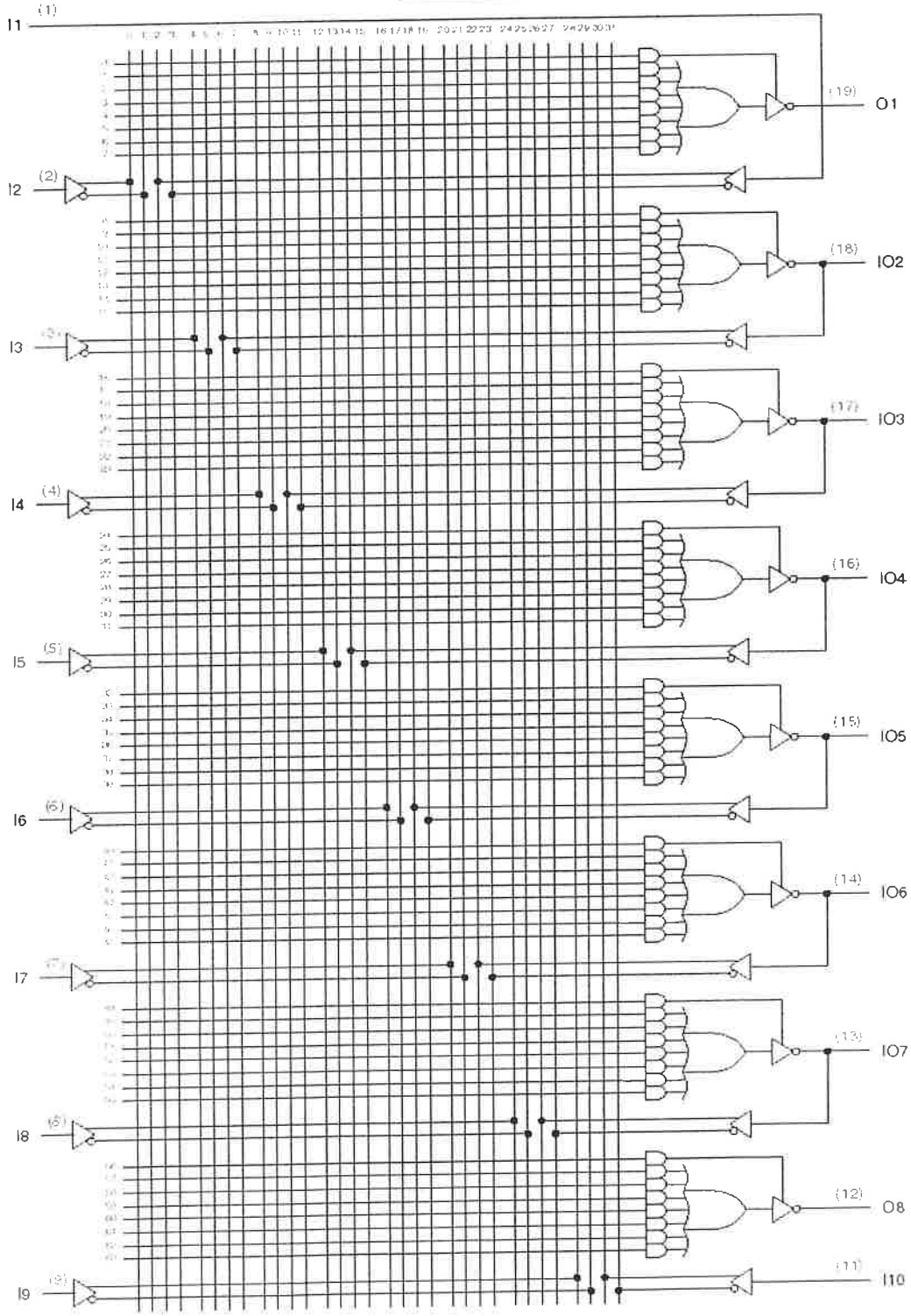
(c) Implement and draw the circuit diagram of the parity generator designed in part (b) showing all the details.

(6 marks)

End of Questions

APPENDIX

PAL16L8



End of Paper