National Exams December 2016

04-BS-8, Digital Logic Circuits

3 hours duration

NOTES:

1. If a doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumptions made with the answer of the question.

2. Candidates may use one of two calculators, the Casio or Sharp approved models. This is a closed book examination; however, candidates are allowed to bring one hand-written information sheet (8.5" X 11") of self-prepared notes.

3. This paper contains **FIVE (5)** questions and comprises **seven (7)** pages.

4. Any **FOUR (4)** questions constitute a complete paper. Only the first four questions as they appear in your answer book will be marked.

5. All questions are of equal marks. Total marks = 100.

6. Each question carries 25 marks and the marks for each part of the questions are indicated in brackets.

7. A PAL16L8 Data sheet is provided in the Appendix. It can be used to provide the solution of Question 3, part (b) and should be attached to your answer sheet.

1. (a) A digital circuit is to be developed that can delay a serial data input signal by 12μsec. Design and implement an economical digital (delay) circuit using flip-flops, gates and any suitable size counters or shift registers if required. The block diagram of the circuit along with its input/output signals is shown in Figure 1. Assume that a 1MHz TTL clock is also available.
Show your complete design with full details including the logic gates, flip-flops, counters or shift register used.

(17 marks)

(b) Justify that the delay circuit designed in part (a) uses minimum amount of hardware. Identify at least two useful applications of the delay circuit.

(8 marks)

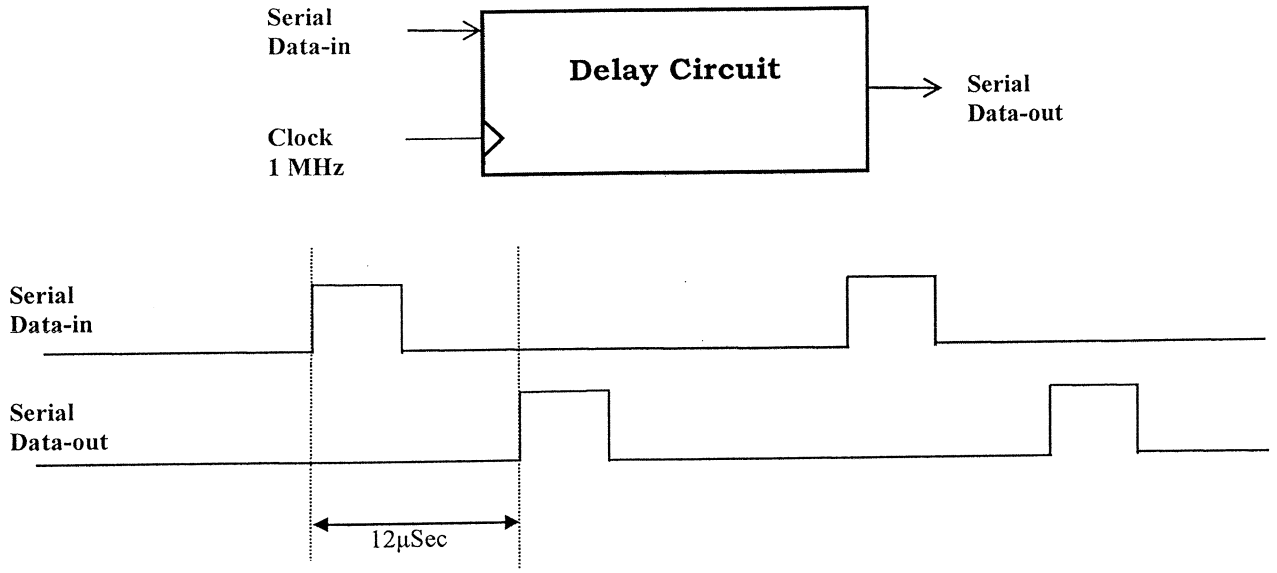


Figure 1

2. (a) Briefly answer the following questions:
- Identify the difference between ripple-carry adder and carry look ahead adder circuits. Describe any reason why a ripple-carry adder takes more time to add as compared with a carry look-ahead adder.
- Determine a BCD representation for $(17{,}000)_{10}$ number. Justify your answer.

(6 marks)

Question #2 continues on Page 3

(b) Determine the number of gates required to implement a 4-bit ripple-carry adder. Use AND, OR and XOR gates only with any number of inputs.

(9 marks)

(c) Show how function **F** can be implemented using minimum number of NAND gates only. Show your complete work related to combinational logic simplification such as K-maps, etc.
F(w, x, y, z) = $\sum$m(0, 2, 3, 5, 6, 13)

(10 marks)

3. (a) Design and implement a memory control logic circuit using the minimum number of suitable size decoder(s) and logic gates. The circuit must generate ten (Q0--- Q9) active low outputs (enable signals) depending on five inputs shown in the truth Table 3.

(12 marks)

Table 3

Inputs					Output
Select	Read-Mem	I_2	I_1	I_0	
1	x	x	x	x	none
x	1	x	x	x	none
0	0	0	0	0	Q0, Q8
0	0	0	0	1	Q3, Q5
0	0	0	1	0	Q4
0	0	0	1	1	Q6
0	0	1	0	0	Q7
0	0	1	0	1	Q2
0	0	1	1	0	Q9
0	0	1	1	1	Q1

(b) Implement the logic circuit of part (a) by using a PAL16L8 device. A PAL16L8 data sheet is provided in the Appendix. Show the intact PAL fuses by crossing them in the diagram and attach it to your answer book.

(8 marks)

(c) Compare the implementations in parts (a) and (b) and identify any advantages of using PAL family devices.

(5 marks)

4. Design a finite state machine with two inputs (**a** and **b**) and one output **Z**. The state table of the finite state machine is given below.

Present State	**Next State** ab = 00	01	10	11	**Output Z**
S1	S2	S1	S2	S3	1
S2	S4	S3	S2	S1	1
S3	S2	S3	S1	S4	0
S4	S2	S3	S4	S1	1

(a) Draw the state diagram and identify the type of the sequential machine. Justify your answers.

(7 marks)

(b) Use D-type flip-flops and other logic gates to design the above finite state machine. Show the main details of your design.

(18 marks)

5. (a) How a Toggle flip-flop can be constructed by using a D-type flip-flop and some logic gates. Draw the complete logic diagram of the circuit.

(6 marks)

(b) Design and draw a sequential circuit using edge-triggered S-R flip-flops that produce a 20MHz frequency signal with 50% duty cycle from a 80MHz clock signal with 30% duty cycle.

(7 marks)

(c) A sequential circuit containing an eight-bit shift register is shown in Figure 5. The shift register is loaded with a given binary number. After eight clock cycles, the register has a converted binary number.

(i) Analyze the circuit and identify its main function.

(ii) Justify your answer by loading a binary in the register and its converted value after 8 clock cycles.

(12 marks)

Figure 5 is given on (next) Page 5

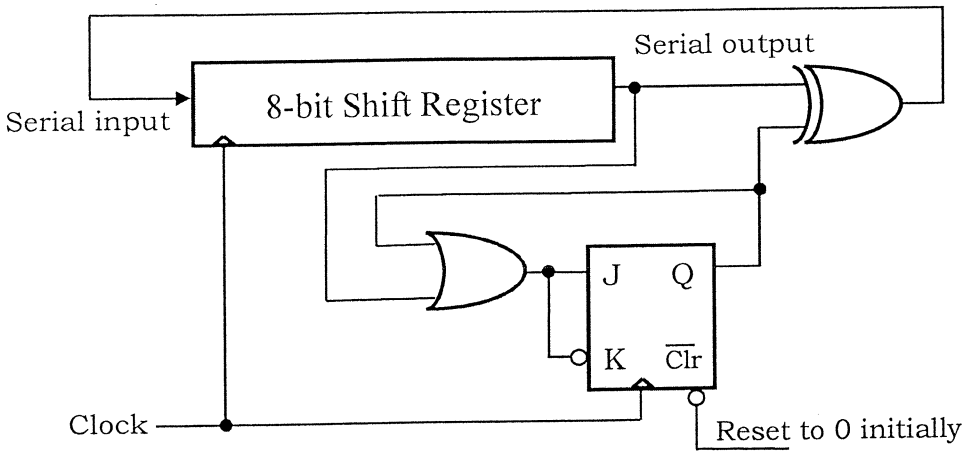
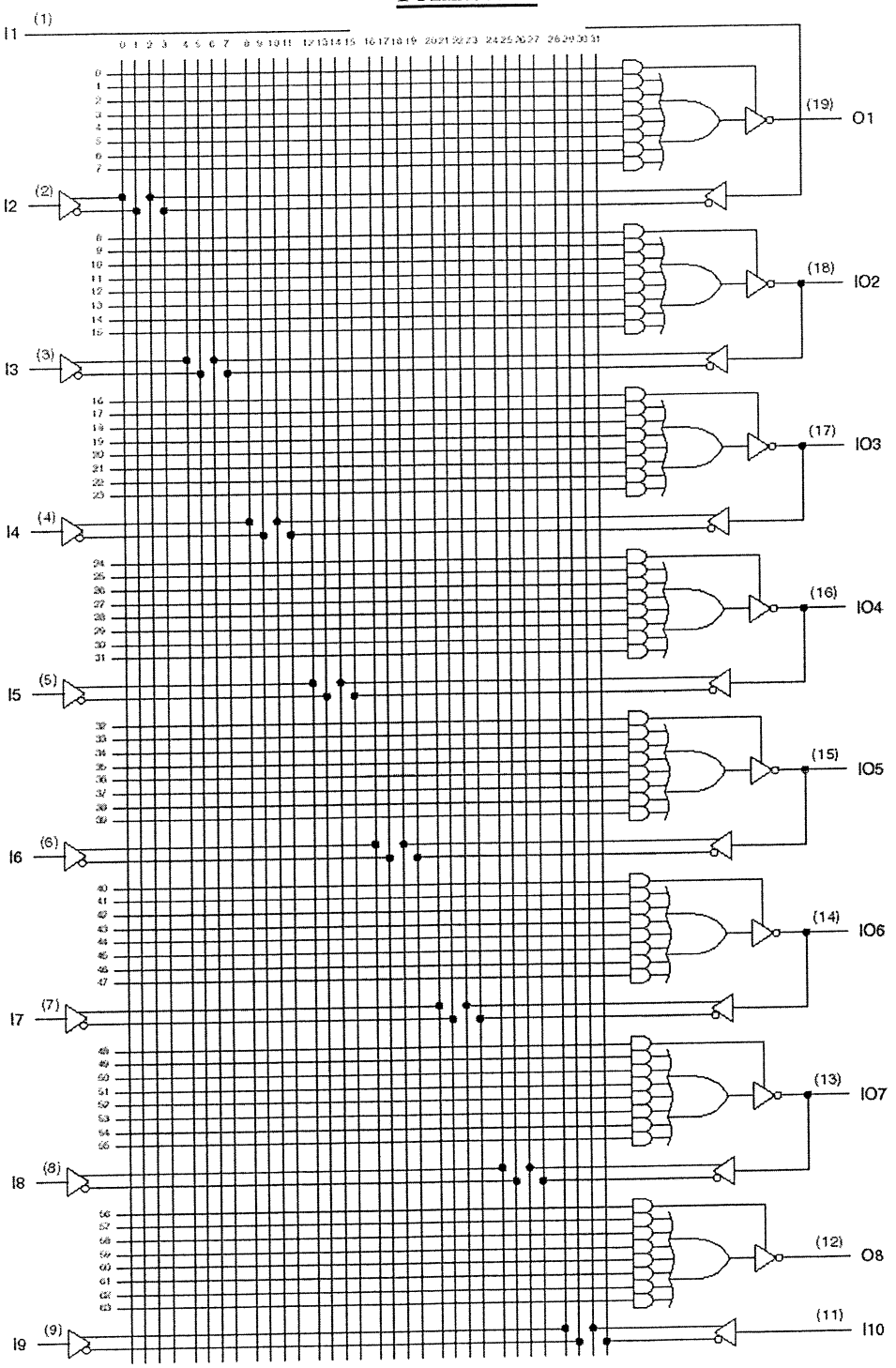

Serial output
8-bit Shift Register
Serial input
J
Q
K
Clr
Clock
Reset to 0 initially

Figure 5

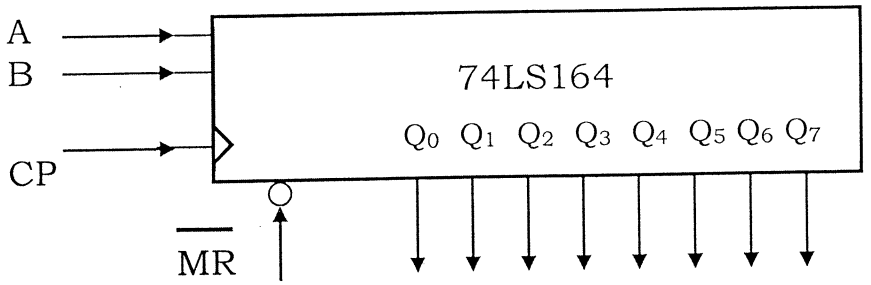
APPENDIX

PAL16L8



Counter and Decoder Data Sheets

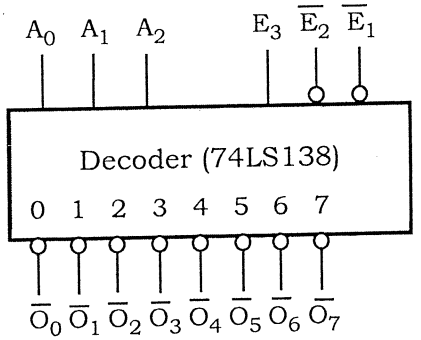
74LS164: 8-bit Shift Register



- An eight-bit shift register with all FF outputs Q_0, Q_1, Q_2, Q_3, Q_4, Q_5, Q_6 and Q_7 are externally available.
- Inputs A and B are ANDED together to produce the serial input to flip-flop Q_0.
- Shift operation occurs at PGTs of the clock input CP.
- The $\overline{MR}$ input resets all FFs asynchronously on a LOW level.

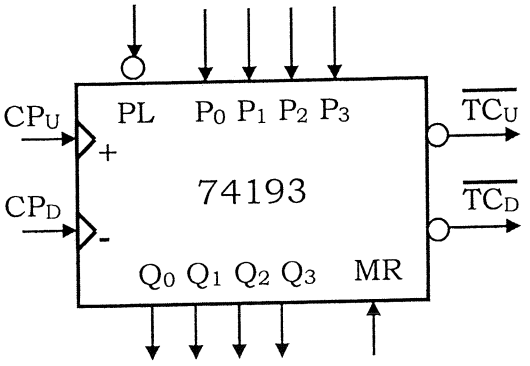
74LS138: 3-to-8 Decoder

Inputs			
$\overline{E}_1$	$\overline{E}_2$	E_3	
0	0	1	Respond to input code $A_2A_1A_0$
1	x	x	Disabled all HIGH
x	1	x	Disabled all HIGH
x	x	0	Disabled all HIGH



74193, 4-bit UP/DOWN Counter

MR	$\overline{PL}$	CP_U	CP_D		Mode
H	x	x	X		Asynch reset
L	L	x	X		Asynch Load
L	H	H	H		No change
L	H	↑	H		Count up
L	H	H	↑		Count down



End of Paper

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Marking Scheme

1. 25 Marks Total
   (a) 17 marks
   (b) 8 marks

2. 25 Marks Total
   (a) 6 marks
   (b) 9 marks
   (c) 10 marks

3. 25 Marks Total
   (a) 12 marks
   (b) 8 marks
   (c) 5 marks

4. 25 Marks Total
   (a) 7 marks
   (b) 18 marks

5. 25 Marks
   (a) 6 marks
   (b) 7 marks
   (c) 12 marks