National Exams May 2013

04-BS-8, Digital Logic Circuits

3 hours duration

NOTES:

1. If a doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumption made with the answer of the question.

2. Candidates may use one of two calculators, the Casio or Sharp approved models. This is a closed book examination; however, candidates are allowed to bring the following into the examination room:
   (i) One hand-written information sheet (8.5" X 11") of self-prepared notes.

3. This paper contains **FIVE (5)** questions and comprises **SIX (6)** pages.

4. Any **FOUR (4)** questions constitute a complete paper. Only the first four questions as they appear in your answer book will be marked.

5. All questions are of equal marks. Total marks = 100

6. Each question carries 25 marks and the marks for each part of questions are indicated in brackets.

7. Data on some relevant Digital ICs are provided in the Appendix. A PAL16L8 Data sheet is provided in the Appendix. It can be used to provide the solution of Problem 1, part (c) and should be attached to your answer sheet.

1. (a) (i) Determine the Boolean expression for output Y of the circuit given in Figure Q1. Simplify the expression using Boolean algebra.

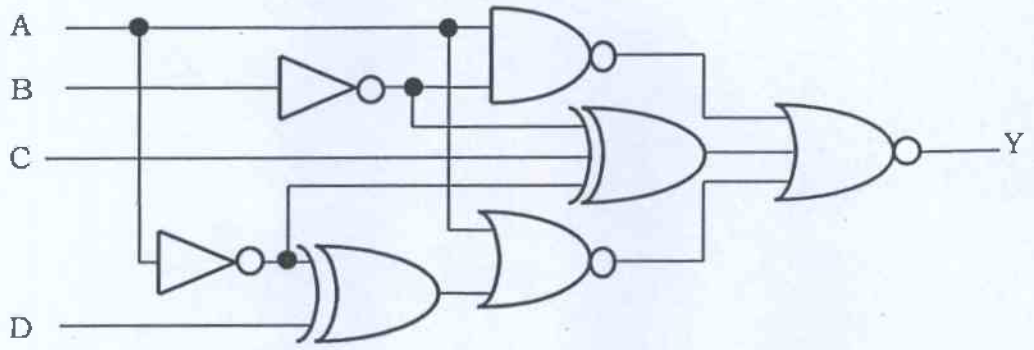


Figure Q1

(ii) Implement the circuit of Figure Q1 using NAND gates only.

(5+7 marks)

(b) Identify the main differences between PAL and FPGA devices.

(6 marks)

(c) Implement the Boolean expression of part (a-i) using a PAL16L8 programmable logic device.

(7 marks)

2. A digital circuit has two outputs Y and Z, whose Boolean functions are given below. Each output has four input variables (a, b, c, d).

$Y(a, b, c, d) = \sum m(0, 2, 4, 6, 7, 9) + D(10, 11)$

$Z(a, b, c, d) = \sum m(2, 4, 9, 10, 15) + D(0, 13, 14)$

(a) Design the minimum cost (gates) using 2-input gates only and assume that the input variables are available in both complemented and un-complemented.

(15 marks)

(b) Compare the cost of the circuit developed in part (a) with the combined cost of two separate circuits implementing Y and Z functions.

(10 marks)

3. (a) Find the 2's complement representation of decimal number -139, where a 10-bit storage is used for 2's complement numbers.

(7 marks)

(b) Design and implement an arithmetic circuit to subtract 8-bit binary numbers by using a 2's complement system. Four-bit parallel adders (e.g. 74LS283) can be employed to implement the subtraction circuit.

(18 marks)

4. (a) Show how a JK flip-flop can be constructed by using a D flip-flop and other logic gates. Draw the complete logic diagram of the circuit.

(7 marks)

(b) A barrel shifter is a shift register that can shift the data by 1 to multiple bit positions. Design a 4-bit Barrel shifter using minimum number of multiplexers, gates and flip-flops that can shift to the left by 0, 1, 2 or 3 positions. Show your complete design work.

(18 marks)

5. Design and implement a sequential circuit to generate parity for a 5-bit serial data. The value of an odd parity is chosen so that the total number of 1s in the coded data group (including the parity bit) is an odd number. Similarly the even parity bit is chosen so that the total number of 1s in the coded data group (including the parity bit) is an even number.

The sequential circuit that generates either odd or even parity depending on a control input EO is shown in Figure Q5. The circuit generates an even parity when EO = 1 and odd parity when EO = 0. The parity generator circuit has a serial clocked data input D_x.

(a) Show your full design by drawing the state diagram and a fully functional sequential circuit with D flip-flops.

(16 marks)

Question No. 5 continues on Page 4

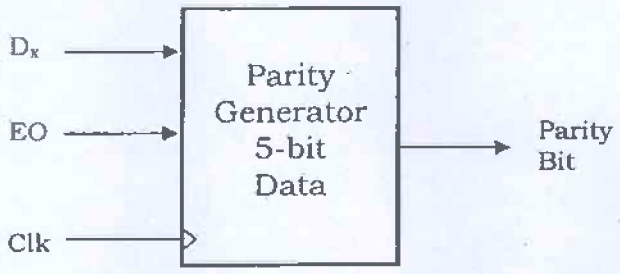


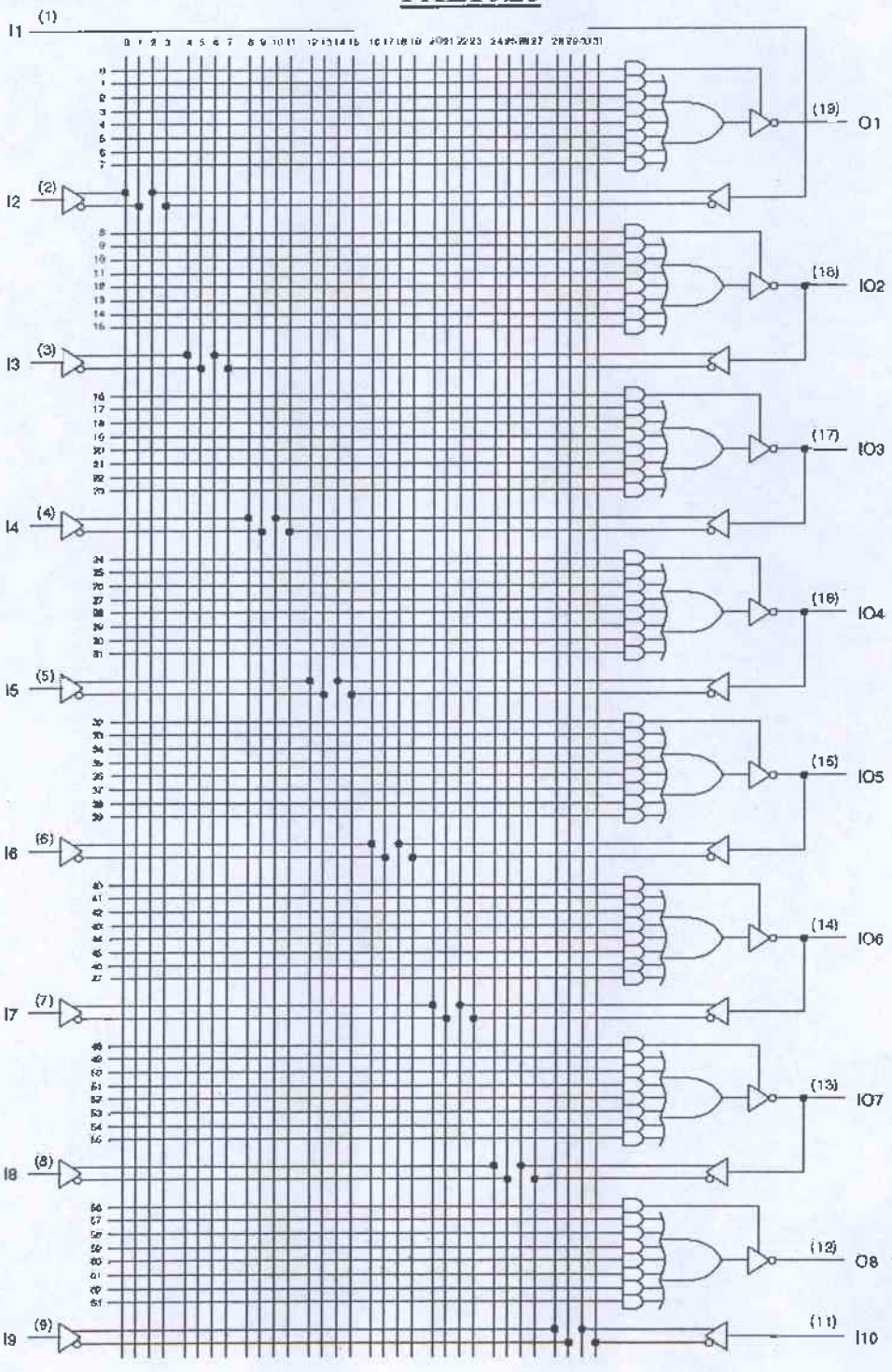
Figure Q5

(b) Suggest any modification in the parity generator circuit of part (a) so that the circuit can be used for checking the parity of an incoming 5-bit datum along with its parity.

(9 marks)

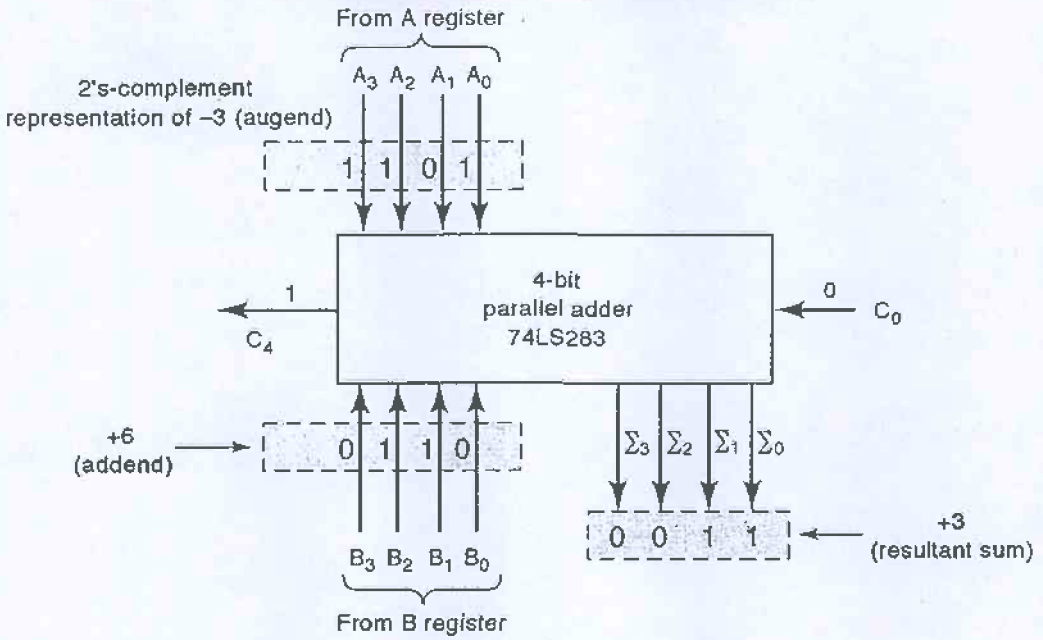
APPENDIX

PAL16L8



Other Data Sheets

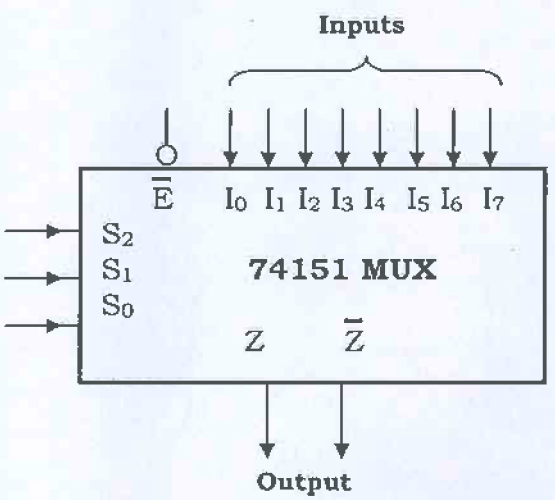
74LS283: 4-bit Parallel Adder



74151 8-to-1 Multiplexer

Inputs Outputs

$\overline{E}$	S_2	S_1	S_0		Z	$\overline{Z}$
H	x	x	x		H	L
L	L	L	L		$\overline{I_0}$	I_0
L	L	L	H		$\overline{I_1}$	I_1
L	L	H	L		$\overline{I_2}$	I_2
L	L	H	H		$\overline{I_3}$	I_3
L	H	L	L		$\overline{I_4}$	I_4
L	H	L	H		$\overline{I_5}$	I_5
L	H	H	L		$\overline{I_6}$	I_6
L	H	H	H		$\overline{I_7}$	I_7



End of Paper