National Exams May 2018

04-BS-8, Digital Logic Circuits

3 hours duration

NOTES:

1. If a doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper. A clear statement of any assumption made with the answer of the question.

2. Candidates may use one of two calculators, the Casio or Sharp approved models. This is a closed book examination; however, candidates are allowed to bring one hand-written information sheet (8.5" X 11") of self-prepared notes both side of the sheet.

3. This paper contains **FIVE (5)** questions and comprises **FOUR (4)** pages.

4. Any **FOUR (4)** questions constitute a complete paper. Only the first four questions as they appear in your answer book will be marked.

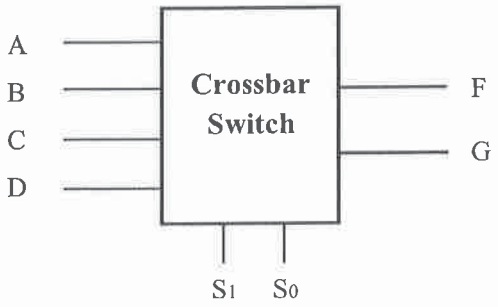
5. All questions are of equal marks. Total marks = 100.

6. Each question carries 25 marks and marks for each part of the question are indicated in brackets.

1. (a) Provide a brief answer with justification. Let A = 1, B = 0, and C = 0, find **X,** where $\mathbf{X} = \overline{(A \oplus B)} \oplus C + A \cdot C$

(5 marks)

(b) Consider the implementation of a circuit with four data inputs (A, B, C, D), two outputs (F, G) and two control inputs (S1, S0). The block diagram and functional truth table of the circuit are given below. Assume that S1, S1', S0 and S0' are available.



S1	S0	F	G
0	0	A	D
0	1	B	C
1	0	C	B
1	1	D	A

Figure Q1

(i) Draw the schematic of the circuit using AND & OR gates only.

(ii) Show the schematic of the circuit using 2-input NAND gates only.

(12+8 marks)

2. (a) Describe the main architectural features of FPGA devices that make these devices versatile when compared with PLA and PAL devices.

(6 marks)

(b) Design and implement a digital circuit that converts 4-bit 2's complement numbers to 4-bit sign-magnitude representation numbers (ranging from -7 to +7). The circuit has four inputs (C_3, C_2, C_1, C_0) and four outputs (M_3, M_2, M_1, M_0).

Show your complete work including the truth table and K-map based simplification. Your overall circuit design must employ the minimum number of 2-input gates.

(12+7 marks)

3. Design a clocked synchronous finite state machine with input A and output X. The output will be asserted (for one clock cycle) whenever the input sequence (serial data) ...1100... has been observed, after a sequence of three or more consecutive zeros i.e. ...000...
A typical sample of the input data A and output X are given below (note the position of X=1 assertions):

A: 0001100001101101000000110000011001100011000 1...
X: 0000010100000000000000000010000001000000010...

(a) Draw the state diagram having minimum number of states.

(7 marks)

(b) Design and implement the synchronous finite state machine by using the flip-flops and logic gates of your choice.

(18 marks)

4. (a) Design a T flip-flop by using a JK flip-flop and other logic gates. Show the complete logic diagram of the flip-flop.

(5 marks)

(b) Synthesize and analyze the counter circuit of Figure Q4, where the NAND gate is used to detect a particular state of the circuit.

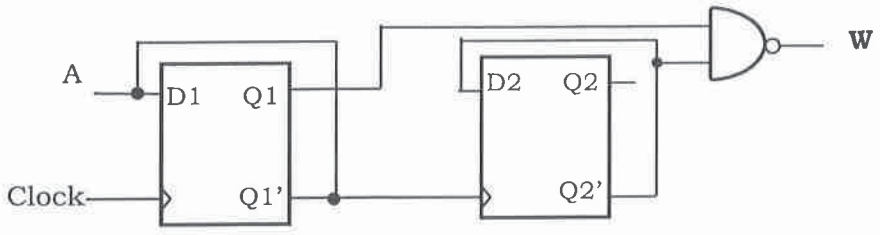


Figure Q4

(i) Is the above circuit a synchronous sequential circuit (Yes or No)? Justify you answer.

(5 marks)

(ii) Identify the circuit state that is detected by the NAND gate.

(5 marks)

Question No. 4 continues on Page 4

(iii) Draw the waveforms of outputs Q1, Q2 and W for a 10 MHz clock. Assume that both flip-flops are initially reset to 0 and the propagation delay of the flip-flop and NAND gate is 10 and 5nsec respectively.

(10 marks)

5. (a) Briefly explain a Barrel shifter by listing its three advantages and/or applications.

(7 marks)

(b) Design a digital system that implements the barrel shifter function. The system has 4 data inputs (D3, D2, D1, D0), 4 data outputs (Q3, Q2, Q1, Q0), and 2 control inputs (S1, S0) as shown in Figure Q5. The control inputs specify the number of positions to shift the input to the left. Inputs that "fall off the end" are rotated around to the low-order bits of the output.

For example, when S1=S0=0, the inputs are simply gated through to the outputs: Q3=D3, Q2=D2, ..., Q0=D0. When S1=0 and S0=1, the input bits are shifted one place towards the left i.e. Q3=D2, Q2=D1, Q1=D0, Q0=D3. Note that D3 is rotated around to the 0th output position. When S1=S0=1, the input is shifted three positions to the left, with the high-order bits wrapping around to the low-order output positions: Q3=D0, Q2=D1, Q1=D2, Q0=D1.

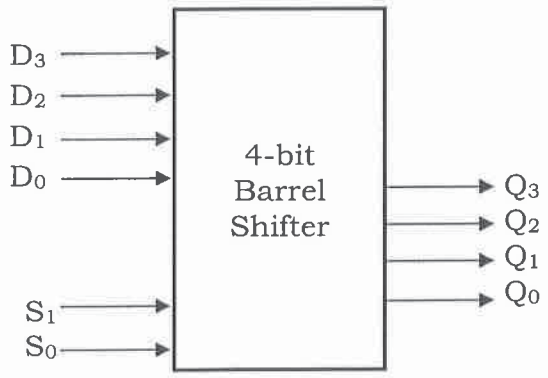


Figure Q5

The easiest way to implement the 4-bit barrel shifter is to use some suitable MSI devices rather than gates.

(18 marks)

(End OF Paper)