National Exams May 2018

17-Phys-A5-B Analog and Digital Electronic Circuits

3 hours duration

NOTES:

1. If doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumptions made.

2. This is an OPEN BOOK EXAM.
   Any non-communicating calculator is permitted.

3. Answer all SIX (6) questions.

4. Please start each question on a new page and clearly identify the question number and part number, e.g. Q1(a).

5. If questions require an answer in essay format, clarity and organization of the answer are important. Provide block diagrams and circuit schematics whenever necessary.

Marking Scheme

1. 15 marks
2. (a) 10 marks; (b) 10 marks;
3. (a) 10 marks; (b)10 marks
4. 15 marks
5. (a) 5 marks; (b) 10 marks
6. (a) 10 marks; (b) 5 marks

Question 1

In the circuit shown in Fig.1 assume V_{BE}= 0.7V, β=100 and neglect Early effect ($V_A = \infty$) for all transistors. R_1= 2 kΩ and R_2= 3 kΩ.

(a) Calculate I_{C1}, I_{C2} and I_{C3}.

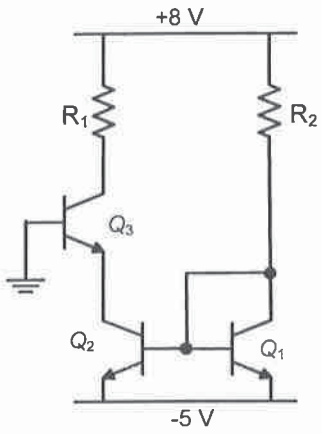

Fig.1

Question 2

Consider the circuit shown in Fig.2. R_1= 2 kΩ, R_2= 15 kΩ, R_3= 5kΩ, R_4= 1kΩ, C_1= 100pF, and C_2= 100nF

(a) Derive the expression for the voltage gain, v_o/v_i. Assume an ideal Op-Amp.
(b) Sketch the Bode plot (dB vs frequency in rad/sec) for the magnitude of the transfer function, v_o/v_i.

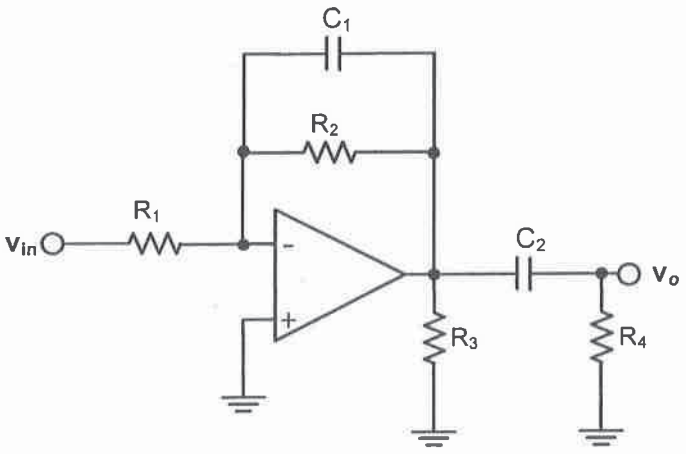

Fig. 2

Question 3:

Figure 3 shows a common source amplifier using PMOS transistor M_1. Consider I_{bias} = 1mA, I_{D3} = 1mA, and C_L = 50fF, Assume all transistors are in saturation region and that $(\frac{W}{L})_1 = (\frac{W}{L})_2 = 4.(\frac{W}{L})_b = 40.(\frac{W}{L})_3 = 80$, $\mu_n C_{ox} = \mu_p C_{ox} = 100\mu A/V^2$, $V_{An} = |V_{Ap}| = \infty$ ($r_{on} = r_{op} = \infty$), C_{gs}=50fF and C_{gd}= 20fF for all the transistors.

(a) Calculate the low frequency gain $A_v = v_o/v_{sig}$.
(b) Calculate the bandwidth (the 3-dB frequency) of this amplifier.

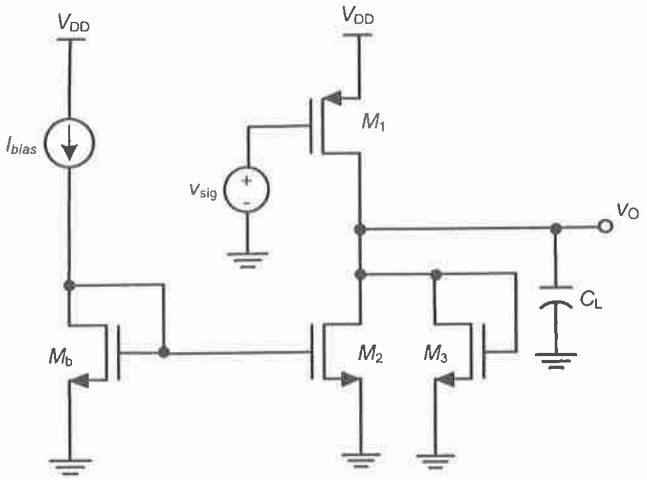

Fig. 3

Question 4

For the amplifier, in Fig. 4, it is desired to obtain a precise gain v_O/v_S using feedback. Assume that $g_{m1} = g_{m2} \neq g_{m3}$, and $r_{o1} = r_{o2} = r_{o3} = \infty$. I_{bias} is an ideal current source. Assume all transistors are in saturation region.

(a) Use the methods of feedback analysis to find the expression of the gain v_O/v_S.

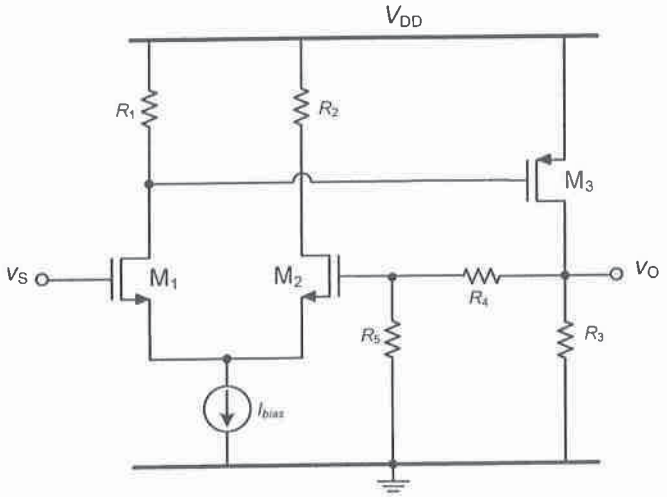

Fig. 4

Question 5

Consider the 4-bit digital-to-analog converter (DAC) using a binary-resistive ladder as shown in Fig. 5. Assume an ideal Op-Amp and R_f=R/2.

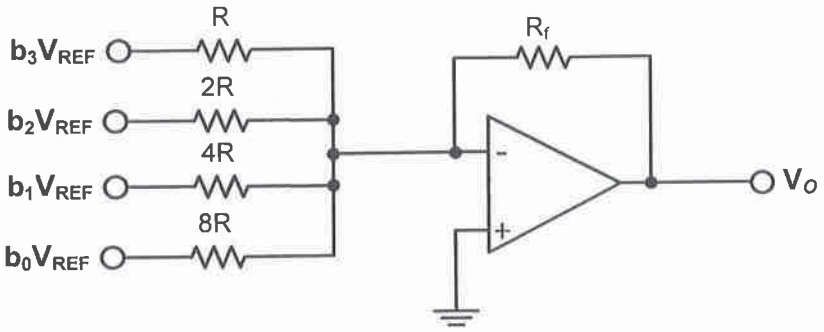

Fig. 5

(a) Find the expressions of the output voltage V_O
(b) Calculate V_O when R = 10kΩ, V_{REF} = 10 V and the applied binary word is 1101.

Question 6

The circuit in Fig.6 shows the pull-up network (PUN) of a CMOS logic gate that implements the function Y.

(a) Find the pull-down network (PDN) that corresponds to the PUN shown in Fig. 6 and hence the complete CMOS logic circuit. Explain your work.
(b) Write the Boolean function realized.

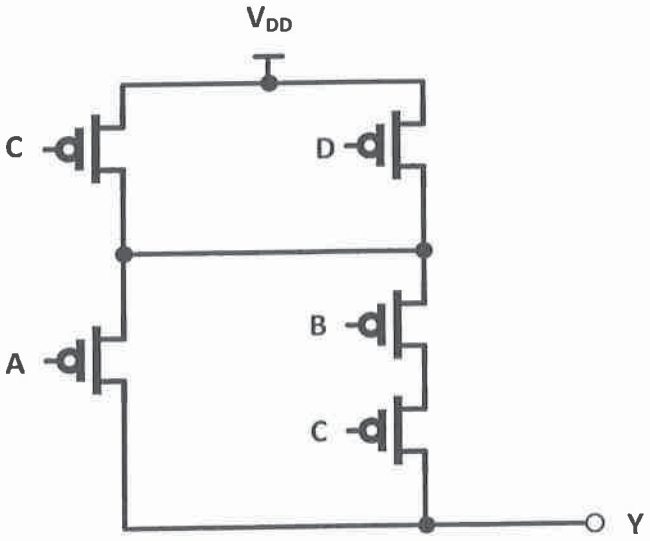

Fig.6