National Exams December 2017

98-Comp-A1, Electronics

3 hours duration

NOTES:

1. If doubt exists as to the interpretation of any question, the candidate is urged to indicate, with the answer, a clear statement of any assumptions made.

2. This is an OPEN BOOK exam.
   Any non-communicating calculator is permitted.

3. FIVE (5) questions constitute a complete exam paper.
   The first 5 questions as they appear in the answer book will be marked.

4. Each question is of equal value.

Marking Scheme

1. 20 marks total (4 parts, 5 marks each)
2. 20 marks total (4 parts, 5 marks each)
3. 20 marks total (4 parts, 5 marks each)
4. 20 marks total (4 parts, 5 marks each)
5. 20 marks total (4 parts, 5 marks each)
6. 20 marks total (4 parts, 5 marks each)
7. 20 marks total (4 parts, 5 marks each)

Question 1 (20 marks)

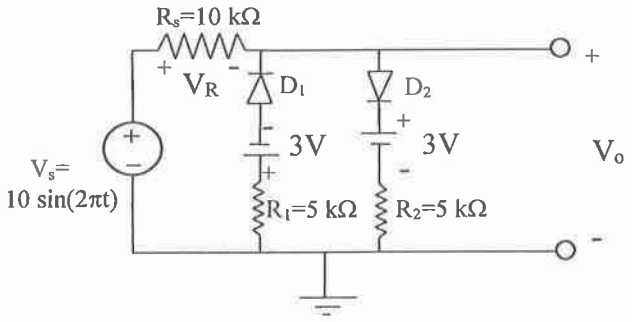

Figure 1. All diodes have a forward voltage drop V_D=0.7V.

The circuit shown in Figure 1 is in steady state:

a) Find an expression for V_o as a function of V_s when D_1 is in forward bias.
b) Sketch V_s and V_o as a function of time, indicating peak voltages.
c) Sketch V_R, as a function of time, indicating peak voltages.
d) Which resistor has the largest peak power dissipation? What power rating would you choose for this resistor?

Question 2 (20 marks)

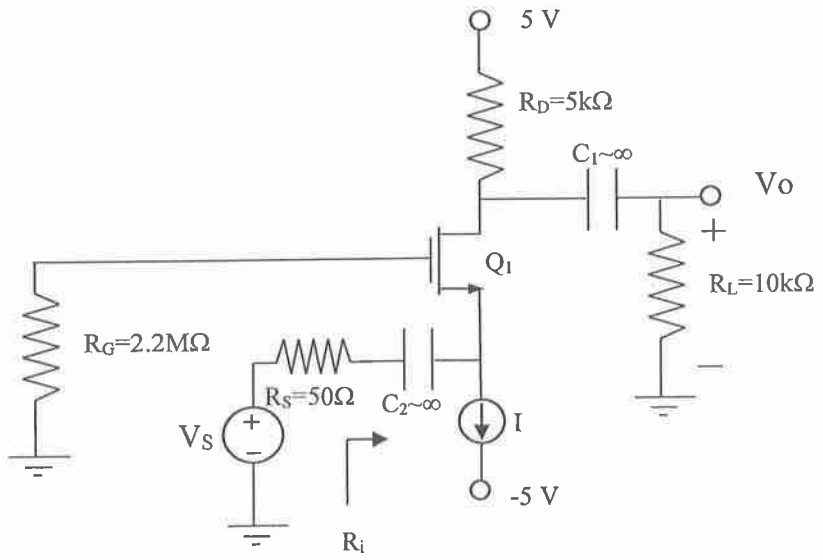

Figure 2. I=500 μA, $k_n'(W/L)$=1 mA/V^2, $|V_t|$=1.5V, V_A=75V

For the circuit shown in Figure 2:

a) Find V_D, V_G, and V_{GS}.
b) Draw a small signal equivalent circuit and find the model parameter values.
c) Find the input and output resistances of the circuit.
d) Find the open circuit voltage gain for the amplifier and the loaded voltage gain.

Question 3 (20 marks)

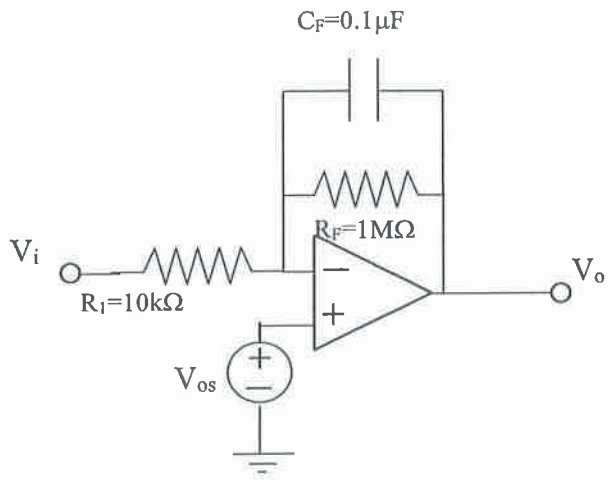

Figure 3. The operational amplifier saturates at +/- 10V. The DC input offset voltage, V_{os} as shown is 10mV.

For the circuit shown in Figure 3:

a) Find the circuit DC gain.
b) Find the circuit AC gain.
c) Sketch the frequency response of the circuit. Find the 3dB frequency and unity gain bandwidth for this circuit.
d) What is the effect of the input offset on the available output voltage swing?

Question 4(20 marks)

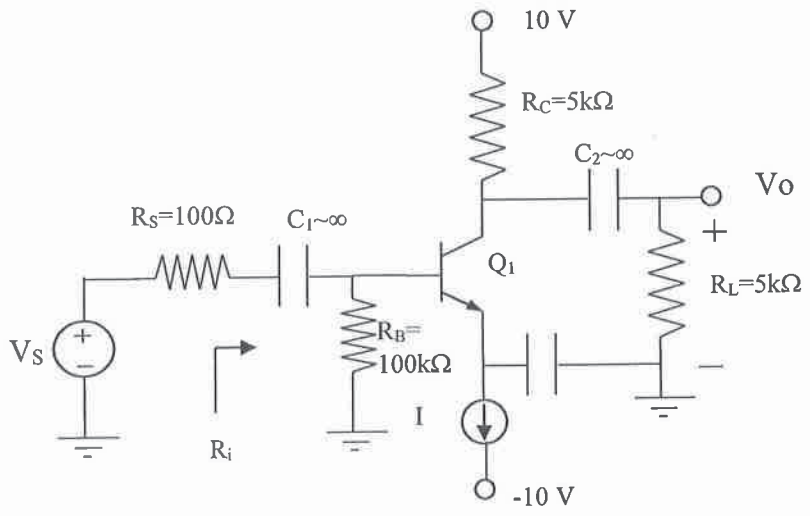

Figure 4. I=1mA, β=100, V_A=100V, V_T=25mV.

For the circuit shown in Figure 4:

a) Find V_C, V_B and V_E.
b) Draw a small signal equivalent circuit and find the model parameter values.
c) Find the small signal input resistance R_i and output resistance Ro.
d) Find the open circuit voltage gain for the amplifier and the loaded voltage gain.

Question 5 (20 marks)

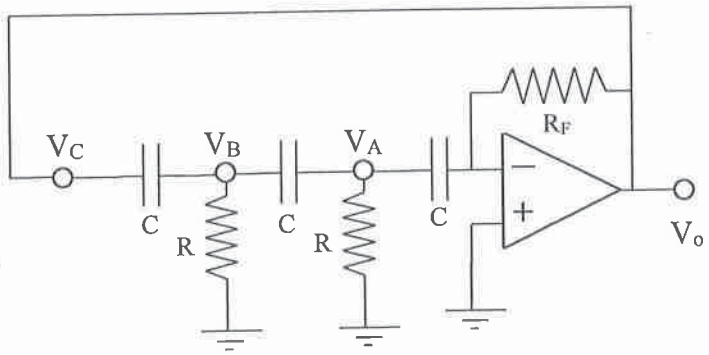

Figure 5. R=10kΩ, C=15 nF

For the circuit shown in Figure 5:

a) Find expressions for voltages V_A and V_B.
b) Find an expression for the loop gain V_o/V_C.
c) At what frequency would the circuit oscillate?
d) What value of R_F would cause oscillation?

Question 6 (20 marks)

Consider a CMOS technology in which an inverter with a minimum gate length L=0.5 μm has a symmetric transfer function for NMOS W/L = 1.5 and PMOS W/L =6.

a) Write a Boolean expression for a 3 input NOR gate and sketch the transistor level gate schematic.
b) Specify sizes (W/L) for all transistors in order to achieve current-driving capability equal to that of the basic inverter.
c) Repeat a) and b) for a three input NAND gate.
d) For the NAND gate in c), find the ratio of maximum to minimum available current to charge and discharge a load.

Question 7 (20 marks)

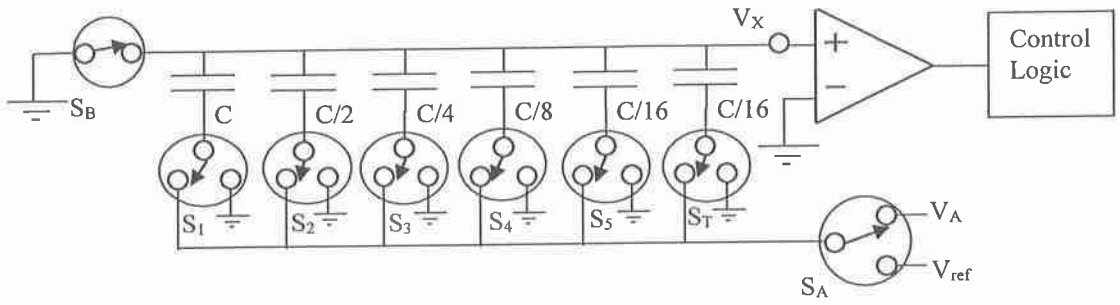

Figure 6.

For the circuit shown in Figure 6, initially S_B is closed (ground) and the capacitors are connected to V_A through S_1-S_5, S_T, and S_A as shown. At t=0 S_B is opened, S_T and S_1-S_5 are connected to ground, and S_A is connected to V_{ref}=4V.

a) What is the voltage at V_X just after t=0?

b) If switch S_5 is connected to V_{ref} while S_T and S_1-S_4 connect to ground, what is the change in V_X?

c) Sequentially connecting capacitors to V_{ref} can be used to generate a binary representation of V_A. What is the full scale voltage that can be converted? What is the resolution of the conversion?

d) If input V_A=1.5 V, which switches will be high (connected to V_{ref}) when conversion is complete?